TKK Dissertations 251
Espoo 2010

INTEGRATED RF OSCILLATORS AND LO SIGNAL GENERATION CIRCUITS

Doctoral Dissertation

Kari Stadius

Aalto University
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Doctoral dissertation for the degree of Doctor of Science in Technology to be presented with due permission of the Faculty of Electronics, Communications and Automation for public examination and debate in Auditorium S3 at the Aalto University School of Science and Technology (Espoo, Finland) on the 23rd of November 2010 at 12 noon.

Aalto University
School of Science and Technology
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Aalto-yliopisto
Teknillinen korkeakoulu
Elektroniikan, tietoliikenteen ja automaation tiedekunta
Mikro- ja nanotekniikan laitos

Distribution:
Aalto University
School of Science and Technology
Faculty of Electronics, Communications and Automation
Department of Micro and Nanosciences
P.O. Box 13000 (Otakaari 5 A)
FI - 00076 Aalto
FINLAND
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ISBN 978-952-60-3450-8
ISBN 978-952-60-3451-5 (PDF)
ISSN 1795-2239
ISSN 1795-4584 (PDF)
URL: http://lib.tkk.fi/Diss/2010/isbn9789526034515/

TKK-DISS-2835

Multiprint Oy
Espoo 2010

ABSTRACT OF DOCTORAL DISSERTATION	AALTO UNIVERSITY SCHOOL OF SCIENCE AND TECHNOLOGY P.O. BOX 11000, FI-00076 AALTO http://www.aalto.fi
Author Kari Stadius	
Name of the dissertation Integrated RF Oscillators and LO Signal Generation Circuits	
Manuscript submitted 16.6.2010	Manuscript revised 5.10.2010
Date of the defence 23.11.2010	
☒ Monograph	☐ Article dissertation
Faculty Faculty of Electronics, Communications, and Automation Department Department of Micro and Nanosciences Field of research Electronic Circuit Design Opponent(s) Docent Markku Åberg Supervisor Professor Kari Halonen	

Abstract

This thesis deals with fully integrated LC oscillators and local oscillator (LO) signal generation circuits. In communication systems a good-quality LO signal for up- and down-conversion in transmitters is needed. The LO signal needs to span the required frequency range and have good frequency stability and low phase noise. Furthermore, most modern systems require accurate quadrature (IQ) LO signals. This thesis tackles these challenges by presenting a detailed study of LC oscillators, monolithic elements for good-quality LC resonators, and circuits for IQ-signal generation and for frequency conversion, as well as many experimental circuits. Monolithic coils and variable capacitors are essential, and this thesis deals with good structures of these devices and their proper modeling. As experimental test devices, over forty monolithic inductors and thirty varactors have been implemented, measured and modeled. Actively synthesized reactive elements were studied as replacements for these passive devices. At first glance these circuits show promising characteristics, but closer noise and nonlinearity analysis reveals that these circuits suffer from high noise levels and a small dynamic range. Nine circuit implementations with various actively synthesized variable capacitors were done. Quadrature signal generation can be performed with three different methods, and these are analyzed in the thesis. Frequency conversion circuits are used for alleviating coupling problems or to expand the number of frequency bands covered. The thesis includes an analysis of single-sideband mixing, frequency dividers, and frequency multipliers, which are used to perform the four basic arithmetical operations for the frequency tone. Two design cases are presented. The first one is a single-sideband mixing method for the generation of WiMedia UWB LO-signals, and the second one is a frequency conversion unit for a digital period synthesizer. The last part of the thesis presents five research projects. In the first one a temperature-compensated GaAs MESFET VCO was developed. The second one deals with circuit and device development for an experimental-level BiCMOS process. A cable-modem RF tuner IC using a SiGe process was developed in the third project, and a CMOS flip-chip VCO module in the fourth one. Finally, two frequency synthesizers for UWB radios are presented.

Keywords RF IC, VCO, LC oscillator, LO generation, UWB	
ISBN (printed) 978-952-60-3450-8	ISSN (printed) 1795-2239
ISBN (pdf) 978-952-60-3451-5	ISSN (pdf) 1795-4584
Language English	Number of pages xvi + 221
Publisher Aalto University, School of Science and Technology	
Print distribution Aalto University, School of Science and Technology	
☒ The dissertation can be read at http://lib.tkk.fi/Diss/2010/isbn9789526034515/	

VÄITÖSKIRJAN TIIVISTELMÄ	AALTO-YLIOPISTO TEKNILLINEN KORKEAKOULU PL 11000, 00076 AALTO http://www.aalto.fi

Tekijä Kari Stadius

Väitöskirjan nimi

Integroidut RF-oskillaattorit ja LO-signaalin generointipiirit

Käsikirjoituksen päivämäärä 16.6.2010	Korjatun käsikirjoituksen päivämäärä 5.10.2010

Väitöstilaisuuden ajankohta 23.11.2010

☒ Monografia	☐ Yhdistelmäväitöskirja

Tiedekunta Elektroniikan, tietoliikenteen ja automaation tiedekunta
Laitos Mikro- ja nanotekniikan laitos
Tutkimusala Piiritekniikka
Vastaväittäjä(t) Dosentti Markku Åberg
Työn valvoja Professori Kari Halonen

Tiivistelmä

Tässä väitöskirjatyössä on kehitetty täysin integroituja LC-oskillaattoreita ja ns. LO-signaalin generointipiirejä. Tietoliikenteen lähetinvastaanottimissa LO-signaali tarvitaan varsinaisen signaalin ylös- ja alassekoitukseen. LO-signaalin tulee kattaa haluttu taajuusalue ja sillä tulee olla hyvä taajuusstabiilisuus ja matala vaihekohina. Lisäksi nykyaikaiset tietoliikennejärjestelmät vaativat tarkkaa kvadratuurista (IQ) LO-signaalia. Näiden haasteiden pohjalta tässä työssä on kehitetty LC-oskillaattoreita, integroituja keloja ja säädettäviä kapasitansseja, ja piirejä IQ-generointiin ja taajuuskonversioihin sekä toteutettu useita kokeellisia integroituja piirejä. Integroidut reaktiiviset elementit ovat tärkeitä hyvän LC-oskillaattorin toteutukseen, ja työssä on kehitetty näiden komponenttien rakennetta ja mallitusta. Yli neljäkymmentä testikelaa ja kolmekymmentä kapasitanssia on toteutettu, mitattu ja mallinnettu. Aktiivipiirillä syntesoituja reaktiivisia elementtejä on myös kehitetty. Nämä piirit lupaavat paljon, mutta tarkempi analyysi osoittaa niiden kärsivän suuresta kohinasta ja pienestä dynaamisesta alueesta. Yhdeksän aktiiviseen säädettävään kapasitanssiin perustuvaa oskillaattoria on toteutettu. Kolmea menetelmää IQ-signaalin generointiin on analysoitu, ja niitä on käytetty toteutetuissa piireissä. Taajuuskonversiota käytetään välttämään ei-toivottuja kytkeytymisiä tai lisäämään saavutettavia taajuuskaistoja. Tarvittavia taajuuskertojia, jakajia, ja sekoittimia on tutkittu, ja lisäksi työssä esitetään patentoitu menetelmä LO-signaalin generointiin WiMedia UWB järjestelmään sekä taajuuskonversiopiiri digitaaliseen jaksonajan synteesipiiriin. Väitöskirjan loppuosassa esitetään tuloksia viidestä tutkimusprojektista. Ensimmäisessä kehitettiin lämpötilakompensoitu GaAs MESFET VCO. Toisessa kehitettiin passiivikomponentteja ja oskillaattoreita BiCMOS prosessilla. Kolmannessa projektissa kehitettiin RF-vastaanotin kaapelimodeemiin käytäen SiGe-teknologiaa. Neljännessä toteutettiin CMOS-oskillaattoreita käyttäen kääntösirutekniikkaa. Lopuksi esitetään kaksi taajuussyntetisaattoria WiMedia UWB radioihin.

Asiasanat integroidut RF-piirit, VCO, LC-oskillaattori, LO-signaalin generointi

ISBN (painettu) 978-952-60-3450-8	ISSN (painettu) 1795-2239
ISBN (pdf) 978-952-60-3451-5	ISSN (pdf) 1795-4584
Kieli Englanti	Sivumäärä xvi + 221

Julkaisija Aalto Yliopisto, Teknillinen korkeakoulu

Painetun väitöskirjan jakelu Aalto Yliopisto, Teknillinen korkeakoulu

☒ Luettavissa verkossa osoitteessa http://lib.tkk.fi/Diss/2010/isbn9789526034515/

Preface

To know is to know that you know nothing.
That is the meaning of true knowledge.
- Confucius -

The work described in this thesis has been done at the Electronic Circuit Design Laboratory of Helsinki University of Technology during many, perhaps too many, years. Despite of the lonely toil, these years have been most interesting and the working atmosphere at the lab deserves special acclaim. Most of the work included in this thesis was done in projects funded by the European Space Agency, the Academy of Finland (SMARAD-2) and the Finnish Funding Agency for Technology and Innovation.

I would like to express my sincerest thanks to Professor Veikko Porra and Professor Kari Halonen for providing me with an opportunity to work at the lab and be involved in research projects as well as in several daily routines. I also wish to thank Professor Jussi Ryynänen for providing challenging research tasks during recent years. During all these years the co-operation and teamwork with several colleagues has been very pleasant and I have learnt a lot of engineering, as well as other, skills from these fellows. In particular, I would like to mention Risto Kaunisto, with whom I shared a workroom for many years. Petteri Alinikula and Jan Holmberg guided me during the first years of my research work. I thank them for all their support. As the years went by I become a senior researcher at the lab and I have had the privilege of working with several talented apprentices in many research projects. I thank all of them for all the hard work and delightful ambience they created in the teams. Finally, I want to express my gratitude to Professor Andrea Lacaita and Professor John Long for pre-examining this thesis.

Anne and Santeri, you are the sunshine of my life.

Kari Stadius

Contents

Symbols

α	Varactor's capacitance range in the SC analysis
α	Amplitude deviation
α	Fitting parameter
β	Fitting parameter
β	Relative capacitance tuning range
β	Capacitance to parasitic capacitance ratio in the SC analysis
Δf	Noise bandwidth
$\Delta\theta$	Phase deviation
$\Delta\omega_{3dB}$	3-dB bandwidth
ε	Van der Pol parameter
ε_0	Permittivity of free space ($8.85 \cdot 10^{-12}$ F/m)
ϕ	Build-in voltage
ϕ	Phase, phase shift, phase deviation
ϕ	Conduction angle
γ	Drain noise coefficient
γ	Grading coefficient (doping factor)
Γ	Impulse sensitivity function
Γ_{dc}	DC component of the impulse sensitivity function
Γ_{eff}	Effective impulse sensitivity function
$\hat{i}_n^2$	Noise spectral density current
$\mathcal{L}$	Phase noise
δ	Gate noise coefficient
δ	Skin depth
σ	Conductivity
μ	Relative permeability
μ	Large Van der Pol parameter
μ_0	Permeability of free space ($4\pi \cdot 10^{-7}$ N/A^2)
μ_n	Surface mobility of the channel for the nMOSFET
θ	Reactance ratio
$\theta_1 \ldots \theta_N$	Signals with sequential phase
τ	Delay
τ	Normalized time
$\hat{v}_n^2$	Noise spectral density voltage
ω	Angular frequency
ω_{osc}	Oscillation frequency
ω_{res}	Resonance frequency
ω_{SR}	Self-resonance frequency
A	Amplitude
A(s)	Transfer function of the amplifying section
a, b	Size factors in the SC analysis
A_{bal}	Amplitude ratio
A_j	Base-emitter junction area
B(s)	Transfer function of the feedback network
BW_{IRR}	Relative bandwidth required for a specific IRR
C	Capacitance

$c(t)$	Time-dependent capacitance
C_{0v}	Capacitance at 0 V bias
c_1, c_2, c_3, c_4, c_5, c_6, c_7, c_8, c_9	Fitting parameters
C_{-3V}	Capacitance at -3 V bias
C_{ave}	Average capacitance
C_{bp}	By-pass capacitor
C_{CH}	Channel region capacitance
C_{db}	Drain-bulk capacitance
C_{ds}	Drain-source capacitance
C_{eff}	Effective capacitance
C_f	Feedback capacitor
C_f	Parallel capacitance in the inductor model
C_{ff}	Fringing field capacitance
C_g	Gyrator capacitance
C_{gb}	Gate-bulk capacitance
C_{gd}	Gate-drain capacitance
C_{gs}	Gate-source capacitance
C_{off}	Off-state capacitance of a SC unit
C_{ox}	Gate oxide capacitance
C_{par}	Parasitic capacitance
C_s	Series capacitor
C_{VAR}	Capacitance of a varactor
C_{vdd}	Supply rail capacitor
d	Distance
D_{in}	Diameter of empty area inside a coil
e	Neper's constant (2.7183)
E_{diss}	Energy dissipated in a resonator
Er, ε_r	Relative permittivity
E_{store}	Energy stored in a resonator
f	Frequency
f_c	Corner frequency
f_m	Offset frequency
f_r	Raster frequency (528 MHz)
f_{sk}	Scaling factor related to skin effect
G	Conductance
G_1, G_2	Parallel conductors for inductors
g_1, g_3, g_5	Polynomial coefficients
g_g	Noise conductance
G_{LS}	Large-signal conductance
g_m	Transconductance
g_o	Output conductance
H	Magnetic field
h_ϕ	Time-variant impulse response
$H(s)$	Transfer function
I, i	Current
i_{act}	Active device current
I_b	Base current
I_{bias}	Bias current
I_c	Collector current
I_d	Drain current

I_{DC}	DC current consumption
K	Process and size parameter of a MOSFET
k	Coupling coefficient
k	Boltzmann constant ($1.38 \cdot 10^{-23}$ J/K)
K_{θ}	Phase detector gain
k_2, k_3	Pole splitting factors
K_{VCO}	VCO tuning gain
L	Inductance
L	Transistor length
L_{eff}	Effective inductance
M	Circuit structure related parameter
M	Mutual coupling
n	Number of stages in a PPF
N	Integer
N_A	Acceptor doping density (n-type material)
N_D	Donor doping density (p-type material)
N_D	Division count
n_i	Intrinsic carrier concentration
NT	Number of turns
P	Population size
P_{DC}	Power consumption
P_{SB}	Relative strength of injected sideband
P_{sig}	Signal power
Q	Quality factor
q	Elementary charge ($1.6 \cdot 10^{-19}$ C)
Q_{ϕ}	Quality factor based on phase response
Q_{11}	Quality factor based on one-port representation
Q_{3dB}	Quality factor based on 3-dB bandwidth
Q_C	Capacitor quality factor
Q_L	Inductor quality factor
q_{max}	Maximum charge swing
r	Growth rate
r_{π}	Base resistance
R_{bias}	Bias resistor
R_C	Capacitor series resistance
$R_{CH,sq}$	Sheet resistance of channel region
R_{crow}	Resistance caused by current crowding
R_d	Drain terminal resistance
R_{DC}	DC resistance
R_{eddy}	Resistance caused by eddy currents
R_{eff}	Effective series resistance
R_G	Resistive part of the generator impedance
R_g	Gate terminal resistance
R_{ind}	Series resistance of an inductor
R_L	Resistive part of the load impedance
R_{on}	On-state resistance of a switch in a SC unit
R_p	Parallel resistance
R_s	Source terminal resistance
R_{sheet}	Sheet resistance
R_{skin}	Resistance caused by the skin effect

S	Signal, signal strength
s	Laplace variable
S	Metal-to-metal spacing
ST	Steepness factor
t	Time
T	Cycle time, period
T	Temperature
t	Metal thickness
u	Normalized voltage
u	Unit step function
v	Voltage
V_{BC}	Base-collector voltage
V_{BE}	Base-emitter voltage
V_{BI}	Built-in voltage
V_{bias}	Bias voltage
V_{cc}	Supply voltage for BJT circuits
V_{dd}	Supply voltage for FET circuits
V_{FB}	Flat-band voltage
V_{GS}	Gate-source voltage
V_{NC}	Voltage region with total negative conductance
V_{osc}	Oscillation amplitude
V_{pp}	Peek-to-peek voltage
V_{TH}	Threshold voltage
W	Transistor width
W	Metal stripe width
X_G	Reactive part of the generator impedance
X_L	Reactive part of the load impedance
y	Admittance
Y	Admittance
Y_i	Input admittance
Y_m	Feedback admittance
Y_o	Output admittance
Z	Impedance
Z_0	Characteristic impedance
Z_g	Active circuit impedance of an oscillator
Z_{gnd}	Ground rail impedance
Z_{sub}	Substrate impedance
Z_{vdd}	Supply rail impedance

Abbreviations

AC	Alternating current
ACL	Amplitude control loop
A/D	Analog to digital (converter)
AIO	Active inductance oscillator
AM	Amplitude modulation
BAL	Balanced (structure / circuit)
BG	Band group
BiCMOS	Bipolar complementary metal oxide semiconductor
BJT	Bipolar junction transistor
BW	Bandwidth
CAD	Computer aided design
CCP	Cross-coupled transistor pair
CD	Common-drain
CG	Common-gate
CMOS	Complementary metal oxide semiconductor
CP	Charge pump
CPE	Common phase error
CT	Center tap
CS	Common-source
dBc	Decibel relative to carrier
DC	Direct current, refers often to frequency = 0 Hz
DCR	Direct conversion receiver
DE	Differential equation
DECT	Digital enhanced cordless telecommunications
DFET	Depletion-mode GaAs MESFET
DFF	Delayed flip-flop
DLL	Delay-locked loop
DOCSIS	Data over cable system interference specification
DPS	Direct period synthesizer
DUT	Device under test
DVB-S	Digital video broadcasting - satellite
ECL	Emitter-coupled logic
EFET	Enhancement-mode GaAs MESFET
EM	Electro-magnetic (field)
ESD	Electrostatic discharge
FC	Frequency converter
FET	Field effect transistor
FFT	Fast Fourier transformation
FM	Frequency modulation
FOM	Figure of merit
Freq	Frequency
GaAS	Gallium arsenide
GPS	Global positioning system
GSM	Global system for mobile telecommunications
GX	Excess gain
HBT	Hetero-junction bipolar transistor
HD2	Second order harmonic distortion
HEMT	High electron mobility transistor

HF	High frequency
IC	Integrated circuit
ICI	Inter-carrier interference
ICO	Current controlled oscillator
IEEE	Institute of electrical and electronics engineers
IF	Intermediate frequency
ILO	Injection locked oscillator
I/O	Input - output
IPD	Integrated passive device
IQ	In-phase quadrature-phase
IRR	Image reject ratio
IS54	Interim standard 54
ISF	Impulse sensitivity function
IV	Current - voltage
LC	Inductor capacitor
LF	Low frequency
LNA	Low noise amplifier
LO	Local oscillator
LTE	Long term evolution
LTI	Linear time invariant
MB	Multi-band
MESFET	Metal semiconductor field effect transistor
MMIC	Monolithic microwave integrated circuit
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
MUX	Multiplexer
N/C	Noise to carrier
NMOS	N-channel metal oxide semiconductor field effect transistor
NPN	n-type p-type n-type (bipolar transistor with p-doped base)
OFDM	Orthogonal frequency division multiplexing
PFD	Phase frequency detector
PLL	Phase locked loop
PML	Philips microwave Limeil
PMOS	P-channel metal oxide semiconductor field effect transistor
PPF	Poly-phase filter
PVT	Process, voltage, temperature
QPSK	Quadrature phase-shift keying
RBW	Resolution bandwidth
RC	Resistor capacitor
RF	Radio frequency, typ. 1 – 10 GHz in this context
SAW	Surface acoustic wave
SC	Switched capacitor
SCA	Switched capacitor array
SCL	Source coupled logic
SE	Single ended
Si	Silicon
SiGe	Silicon germanium
SMD	Surface mounted device
SNR	Signal to noise ratio
SOI	Silicon on insulator

S-par	Scattering parameters
SPICE	Simulation program with integrated circuit emphasis
SSB	Single sideband
SST	Steady state
SX	Frequency synthesis / synthesizer
THD	Total harmonic distortion
TI	Texas Instrument
TKK	Helsinki University of Technology
TLT	Transmission line transformer
TR	Tuning range
UMTS	Universal mobile telecommunications system
UWB	Ultra wideband
VCO	Voltage controlled oscillator
VDP	Van der Pol
VG	Virtual ground
VGLNA	Variable gain low noise amplifier
VICO	Variable impedance converter oscillator
VSWR	Voltage standing wave ratio
VTT	Technical research centre of Finland
WLAN	Wireless local area network

1 Introduction

1.1 Background and Motivation

This thesis deals with integrated LC oscillators and LO signal generation circuits. In the mid-1990s silicon IC technologies evolved enough to be used in RF IC circuits with the operating frequency range of 1 – 2 GHz. At the same time new communication systems emerged that required small-sized cost-effective electronics. In the early days of silicon RF ICs there were doubts as to weather we could actually integrate an LC oscillator with a sufficient performance. An understanding of the proper resonator elements – tunable capacitors and coils – was not yet developed and they had a poor performance both because of the limitations of the technology and their non-optimal structures. Furthermore, there was a lack of experience of proper circuit arrangements. However, to be able to integrate a complete LO frequency synthesizer on the same chip as the actual transceiver results in significant savings in power consumption, size, cost and logistical issues. Furthermore, full integration improves reliability. All these issues motivated major research activity on a global scale, and the work presented in this thesis is a small part of that. LC oscillators have a hundred-year-long history and one may wonder why there are still research challenges left. The fundamental reason is that an oscillator is a nonlinear circuit, and we have limited methods to analyze it with symbolic calculus. This is particularly true for oscillator noise analysis. Improvements in computer-aided circuit simulations made detailed noise simulations possible, and these results led to advances in circuit arrangements and in theoretical studies as well. During recent years significant advances have taken place in three major fields. Resonators have reasonably high quality factors and their frequency tuning range is large as well, thanks to improvements in fabrication technology and accumulated knowledge of good device structures. The understanding of good circuit arrangements has improved, and computer-aided simulation methods make detailed circuit simulations possible. Nowadays, good-quality LC oscillators can be integrated, and we can consider the challenge solved for single-system radios, at least from the academic perspective – RF IC oscillator designing is still a hard engineering task. However, in recent years radios have evolved first into multi-band radios, then into multi-system radios, and the forthcoming steps are a true software-defined radio, and eventually a cognitive radio. In these radios the LO signal needs to span a large frequency range and change its frequency quickly, and more than one LO signal is needed concurrently. These requirements call for new innovative techniques in LO signal generation and hence this research field will flourish in the future as well.

1.2 Organization of the Thesis and Research Contribution

The topics of this thesis can be divided into five segments: theoretical issues (Ch. 2), circuit topologies (Ch. 3 – 4), the structure of the LC resonator (Ch. 5 – 7), the post-processing of the oscillator's signal (Ch. 8), and the presentation of some research projects and their results (Ch. 9). Although the actual topic of the thesis is the generation of the LO signal, the thesis mainly focuses on integrated LC oscillators – and for a good reason. I personally have some design experience of all the main blocks of a typical RF transceiver, and among these the LC oscillator is one of the most demanding circuits to design. It is cumbersome from the theoretical point of view, it often has very tight requirements, simulations are tricky, and it employs devices that are rarely used in other circuits. Therefore, most of the material in this thesis deals with LC oscillators. The typical arrangement of the LO signal generation unit, a frequency synthesizer, is to use a phase-locked loop (PLL) to couple the high-frequency oscillator with a high-quality low-frequency reference signal. The LO signal that is generated is thereafter often post-processed in a quadrature-signal generation circuit, or in a frequency

divider. The topics of this thesis are limited to the design of radio-frequency circuits. In particular, the general analysis of PLL properties is advisedly omitted, and the related low-frequency circuits too are just mentioned briefly.

The aim of Chapter 2 is to introduce oscillators and related concepts to the reader and present some slightly theoretical studies. Chapters 3 and 4 represent the most common LC-oscillator topologies and the related analysis. Most of this material can be found in the literature, but the author is able to emphasize many issues that are not generally known and to represent the vital issues in a concise manner. These three chapters also form the background for the actual circuit design projects. Chapter 5 deals with monolithic coils and also, briefly, with bonding wires. The structures and modeling issues of the coils are discussed. During the research work I have implemented, measured with on-wafer probing, and modeled over forty integrated inductors. Some of these results are presented in an appropriate context. I have also performed an extensive amount of electro-magnetic field simulations for modeling inductors, and the results in Chapter 5 demonstrate excellent agreement. Furthermore, an automated simulation procedure was developed. Chapter 6 covers various types of variable capacitors. Device structures, modeling issues and characteristics are discussed. Here as well, the device measurements support the presentation. Both integrated inductors and capacitors have some shortcomings. Chapter 7 presents active circuits that mimic these passive devices. The idea was to replace a passive device with an active counterpart that has a better performance. It turns out that although these circuits show promising characteristics, detailed analysis reveals that these circuits have high noise and poor large-signal properties. In Chapter 8 we finally leave the oscillators. The chapter deals with quadrature signal generation circuits, and techniques for frequency conversion; that is, how the signal is transferred from a certain frequency to another. Two design cases are presented. Finally, Chapter 9 presents five research projects. In the first one I developed a temperature compensated GaAs MESFET VCO. The second project was about passive device and oscillator development with an experimental-level IC process. The third project was a larger entity intended for a cable tuner. I was a project manager leading the circuit development and carrying out the system-level design. I designed all the oscillators, and I also acted as the official master's thesis instructor for three apprentices. In the fourth project I developed a 4-GHz VCO module with a flip-chip technology. The last project described in this thesis was about UWB transceiver development. Here I was responsible for the LO generation, and I designed the related RF circuits. My apprentice designed the phase-locked loops under my guidance.

Some of the material in this thesis has been previously published in journals and at conferences. References are provided when appropriate. For the papers referred to I am the first author of 3 journal papers and 17 conference papers, and correspondingly a co-author of 7 journal papers and 12 conference papers. One patent has been granted and another one is pending.

2 Oscillator Fundamentals

In electrical engineering, an oscillator is a device used for creating a waveform with a desired shape and frequency. It is an apparatus, which produces a periodic signal from a non-periodic source of energy. Either sinusoidal or harmonically rich (square) waveforms are usually desired for high frequency applications. At lower frequencies other waveforms, such as triangular or ramp ones, are applied in various signal processing applications [2.1]. In a voltage-controlled oscillator (VCO), information in voltage form is converted into frequency form. We can even directly modulate the VCO frequency, thus creating a primitive radio transmitter. Though, voltage tuning is usually used for achieving and maintaining the appropriate oscillation frequency. Phase-locked loops (PLL) are exclusively used for this. The main emphasis in this thesis is on VCOs and the tuning is used for setting the desired frequency. Simply speaking, an oscillator is just a circuit with an unstable DC operation point. In such a circuit regenerative situations exist and small fluctuations such as noise or boot-up transients start a growing wave. The oscillation amplitude grows until the boundaries are met and the oscillation swing stabilizes. This limiting function is nonlinear, meaning that all oscillators are fundamentally nonlinear. An unpleasant consequence of this is that linear analysis methods are to some extent inaccurate, and unfortunately, precise nonlinear symbolic analysis methods do not exist. Dynamic systems are mathematically studied in books such as [2.2]-[2.6], but the focus is on mathematical methods and remains mainly qualitative. It is difficult to draw conclusions for practical purposes on the basis of this material. In some cases simplified nonlinear solutions are found but, in general, oscillator design relies heavily on nonlinear computer-aided simulation methods. The purpose of this chapter is to provide background knowledge concerning the subject of this thesis. First, oscillation classification is discussed and various oscillator categories are described. In Section 2.2 a primitive LC oscillator called the van der Pol oscillator is used to demonstrate some nonlinear effects in oscillators. Nonlinear oscillator simulation methods are discussed in Section 2.3 as they play such an important role in oscillator design. The concept of phase noise is presented in the last part of this chapter.

As a general comment it is worth emphasizing that the oscillator designer's task is to create a system with controllable and predictable instability. It is a fairly easy task to create an unstable circuit, but very challenging to create an oscillator with the desired characteristics.

2.1 Oscillator Classification

It is a hard task to classify oscillators, since the structure, behavior, and targeted applications of these circuits vary enormously. The purpose of this section is to briefly introduce various oscillator types and provide some general insights into the focus of this thesis, especially keeping non-expert readers in mind. At least four methods for categorizing oscillators exist. The first one is based on the structure of the oscillator and the second one on the oscillation mode. The third method is to consider the amplitude limitation mechanism. The fourth one is to consider the order of the resonator [2.7]. Furthermore, one might categorize oscillators on the basis of the application that is targeted or on a certain feature, such as frequency range, power level, tuning ability, or noise characteristics.

2.1.1 Oscillator Structure

The simplest way of classification is to study the structure of an oscillator. The three most commonly used monolithic RF oscillator types are depicted in Figure 2.1. These are ring oscillators, emitter-coupled multivibrators, and LC-oscillators. Furthermore, crystal oscillators [2.8]-[2.10] and microwave resonator oscillators [2.11] are also widely used. These resemble LC oscillators and further discussion is therefore omitted. Various RC oscillator types are commonly used at lower frequencies [2.1], [2.7], [2.12].

A four-stage ring oscillator is depicted in Figure 2.1a. Denoting the corresponding delay of an inverter stage by τ, the oscillation frequency is $f_{osc}=1/8\tau$. As a crude estimation, the preceding stage drives the capacitive input load of the following inverter stage and the driving capability depends on the bias current of the stage. Hence, the oscillation frequency can be expressed by

$$f_{osc} = \frac{I}{8 C V_{osc}} \tag{2.1}$$

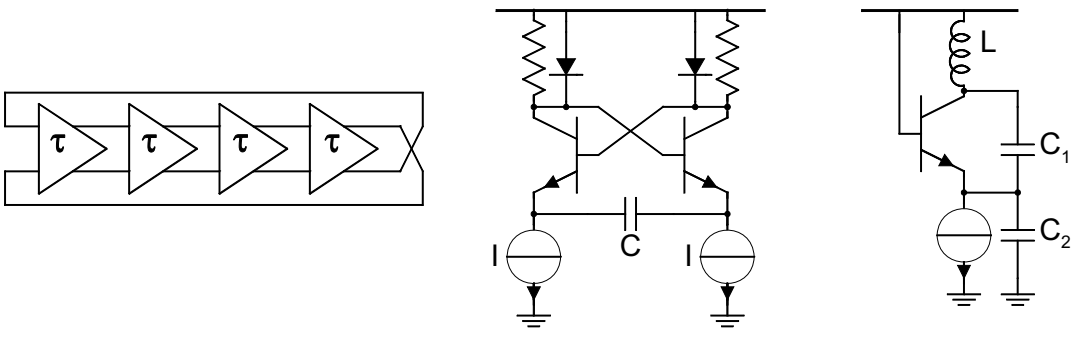
In the early stages of electronic oscillators, strongly nonlinear RC oscillators were often used, and, for instance, Abraham and Bloch developed a circuit in 1919 [2.2] that resembled the emitter-coupled multivibrator shown in Figure 2.1b. In the circuit the left-hand and the right-hand branches conduct alternately in such a way that the capacitor is charged and discharged by the current sources. The circuit provides a symmetrical square wave output across the diodes. The frequency of the oscillation can be expressed as

$$f_{osc} = \frac{I}{4 V_{BE} C} \tag{2.2}$$

Both ring oscillators and emitter-coupled multivibrators share the same characteristics. They are easy to tune over a large frequency range and they do not require inductors. Note that the oscillation frequency depends on currents and voltages, quantities that are naturally influenced by noise. This gives a hint that these oscillators suffer from high phase noise. The unavoidable high phase noise is the reason why LC-oscillators are favored instead of these.

A common-base Colpitts oscillator is depicted in Figure 2.1c. The active device is surrounded by a reactive feedback network (capacitors C_1 and C_2) in such a manner that the circuit is unstable and it oscillates at the frequency

$$f_{osc} = \frac{1}{2\pi}\sqrt{\frac{1}{L\dfrac{C_1 C_2}{C_1 + C_2}}} \tag{2.3}$$



(a) (b) (c)

Figure 2.1. Typical RF oscillators: a) ring oscillator b) multivibrator c) LC oscillator.

2.1.2 Oscillation Mode

Ring oscillators and multivibrators are commonly called relaxation oscillators, although they can also be designed to be weakly nonlinear and to produce almost sinusoidal waveforms. At low frequencies, transistors operate almost like ideal switches, resulting in a piecewise-linear system. At RF frequencies the behavior is significantly smoother. In such a situation these circuits do not necessarily oscillate in the relaxation mode any longer. Thus, classification based solely on the topology of the circuit is not sufficient in itself to describe the circuit. An oscillator can be in one of four modes: mute (no oscillations), harmonic oscillation, relaxation oscillation, or chaotic behavior.

The term harmonic oscillation refers to a sinusoidal waveform found in an ideal undamped second order system, e.g. in an LC resonator. All real oscillators generate distortion. Thus, the term 'harmonic oscillator' refers to a weakly nonlinear oscillator with an almost sinusoidal waveform [2.13]. The amount of distortion present depends on various aspects, such as the limitation mechanism or the structure of the circuit.

As already stated, the previously introduced ring oscillator and multivibrator are commonly called relaxation oscillators. In such a circuit the amplification required for oscillation build-up is far greater than what is needed. The result is that the circuit switches its state in a rapid manner, and between these actions a long period of an almost constant state exist. The term 'relaxation' dates back to the era of vacuum tubes. Vacuum tubes quickly relax (i.e. release) their voltage after slowly building up tension. In the section dealing with the van der Pol oscillator more discussion of these matters is given and it is demonstrated that a simple LC oscillator may behave in relaxation mode as well.

Nature itself is fundamentally a chaotic system, and thus ubiquitous chaos surrounds us. Electronic circuits can also exhibit chaos. Prior to common awareness of chaos, it was called "irregular noise", "multi-oscillation" or "non-periodic oscillation". A perspective on the history of general chaos research is given in e.g. [2.14] and tutorials for electrical engineers were provided in [2.15]-[2.18]. In the past two decades a vast number of papers have been published on this field. Therefore, what follows here is only a cursory glance and advisedly maintains a very general level. Chaos theory is a fairly new field of science and even general definitions, such as what chaos really is, are not fixed. Our previous definition of an oscillator at the beginning of this chapter talks about periodicity, whereas chaotic circuits are non-periodic. Thus, the term 'chaos oscillator' is itself contradictory. If a definition is required, it might be this: a chaotic system creates a non-periodic flow and has a highly sensitive dependence on the initial conditions, and yet it is deterministic. Typically, the behavior of the system depends on the quantity of a certain parameter, often called the bifurcation parameter. In other words, the quality of the system depends on a quantity. This idea differs fundamentally from the principles of classical physics. Prior to going into examples of electrical circuits, I want to present an amazingly simple model, which behaves chaotically. The population biologist Robert May developed this simple discrete-time model for population growth [2.6],[2.14]:

$$P_{n+1} = rP_n(1 - P_n) \tag{2.4}$$

Here, P is the normalized population size and r is the growth rate. It appears that if $1<r<3$ the population size will stabilize, but within values of $3<r<4$ the population size oscillates between levels of two, four, eight etc. and finely confronts chaos. Here a very simple (mathematical) system creates a very complicated set of behaviors. Thus, chaos is not caused by a system having a complicated structure.

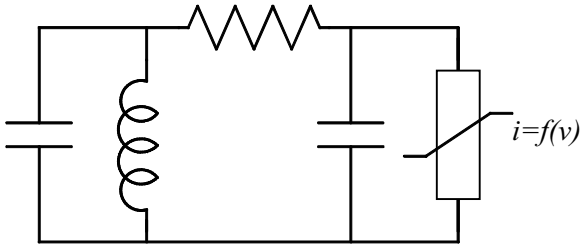


Figure 2.2. Chua's circuit, the simplest electrical chaos generator.

Figure 2.2 shows a real workhorse of electrical chaos circuits, Chua's circuit. It is the choice of a large number of papers dealing with chaos because it is the simplest chaotic circuit, it is easily realizable in a laboratory, and it has a wide repertoire of behavioral modes [2.19]. It is depicted here to emphasize again that a simple system can behave chaotically. In general, a continuous-time system has to be nonlinear and at least third-order to be potentially chaotic. In most examples of chaotic circuits LC oscillators are studied, but chaotic behavior is by no means restricted to these. Moreover, it should be noted that hysteresis increases the dimensions of the system by one [2.20],[2.21], and thus e.g. some RC oscillators, which accidentally include hysteresis, may turn out to be chaotic. A theoretically elegant explanation of chaotic behavior is given by considering bifurcations [2.22]. If an appropriate system parameter (bifurcation parameter) is altered, a stable system undergoes its first bifurcation and a steady oscillation appears (period-1 oscillation). When the system parameter is tuned further, a second bifurcation takes place and the oscillator enters the subharmonic region (period-2 oscillation). After some bifurcations, the system eventually becomes chaotic. In [2.23] a bifurcation diagram for a Colpitts oscillator is given. It reveals that in a typical design case for an ordinary RF oscillator (resonator Q>5 and excess gain<3) the circuit is safely far from the chaotic region. This is in good agreement with practical observation: unwanted chaotic oscillations are rarely met. Figure 2.3 depicts a generalized situation where chaos may exist [2.24],[2.25]. It is important to keep in mind this kind of general scheme if unwanted chaotic behavior is observed and the cause is sought. Here two oscillators try to synchronize to each other. Nonlinear coupling causes that synchronization in harmony does not take place and the two oscillators "fight" with each other, resulting in chaotic behavior. For instance, if the nonlinear coupling network is two diodes connected in antiparallel, the oscillation swing grows in both oscillators independently until the diodes open up. Then the diodes may damp the oscillations, the oscillators feed or pull energy between each other, and indeed a fuzzy situation exists. As an example of chaotic behavior in a simple oscillator circuit, subharmonic and chaotic behaviors in a common-base Colpitts oscillator are depicted in Figure 2.4.

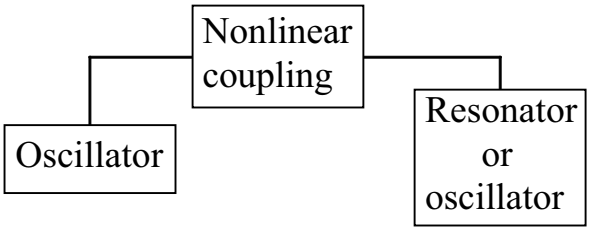


Figure 2.3. Generalized chaotic system.

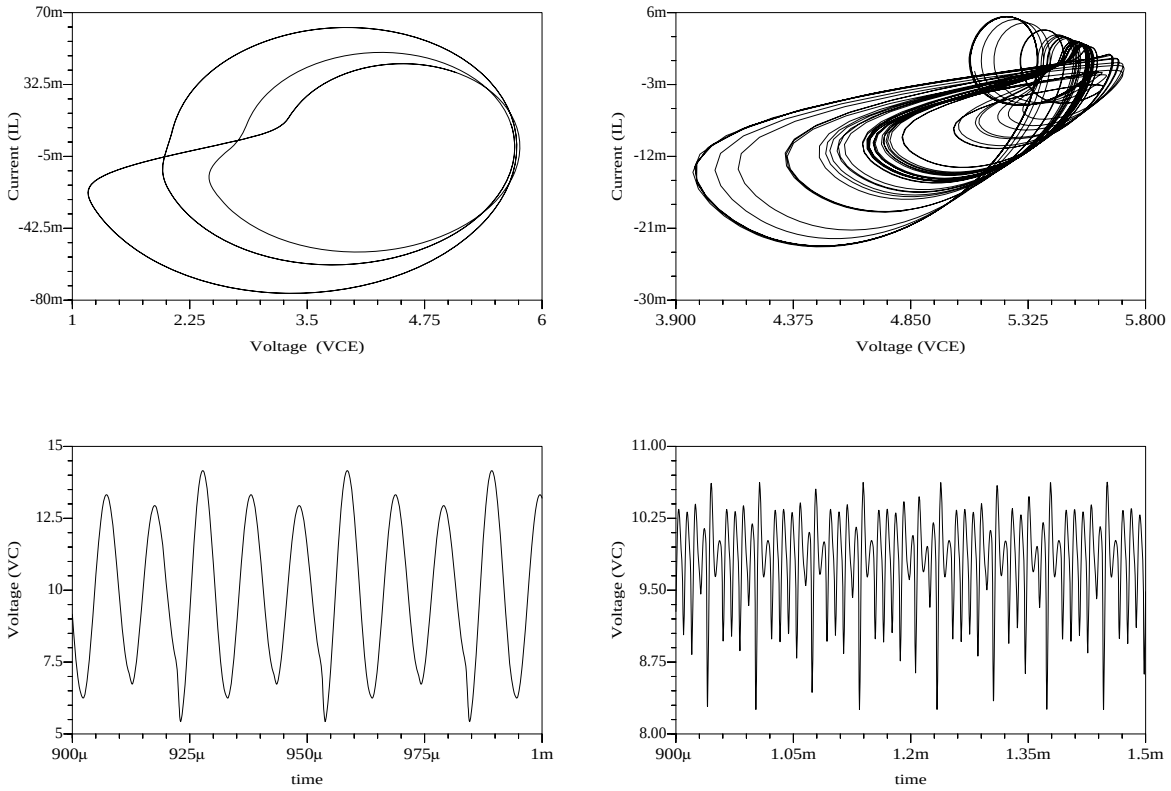


Figure 2.4. Subharmonic (left) and chaotic (right) oscillation in a Colpitts oscillator (Fig. 2.1c).

2.1.3 Amplitude Limitation

All oscillators include an amplitude limitation mechanism. At least four methods exist: a power- sensitive attenuator, self-limiting, automatic amplitude control loop and clipping [2.13].

Power-sensitive attenuators are usually some kind of temperature-sensitive resistors. They provide a design method for low distortion, but the long time constant imposes a limitation on the rate at which the oscillation frequency can be changed [2.13]. Hence, these are rarely used in RF VCO implementations. A nice example of an implementation is the first oscillator of *Hewlett & Packard*, described e.g. in [2.26].

Most RF oscillators are self-limiting; that is, circuits where the limitation of the oscillation amplitude is caused by the nonlinearity of the same device that generates the excess power required to maintain the oscillation. These types of oscillators are almost exclusively used in modern RF and microwave IC implementations since they are simple to construct and the alternatives rarely show better performance. In this thesis too, all the design cases presented are self-limiting.

An amplitude control loop (ACL) can be used if a particularly low distortion or constant output amplitude over the tuning or drift of parameters is desired. The conceptual system is depicted in Figure 2.5. Here an amplitude detector provides a control voltage, which is compared to the desired level *Vref*, and the oscillator bias current is tuned correspondingly. The ACL technique ensures a fast and reliable start-up with an eventually low distorted output. Its drawbacks are the increased noise caused by the control loop, the increased complexity, and the slightly

increased power consumption. Furthermore, the control loop itself may be unstable [2.27]. Some ACL case studies are reported in [2.28]-[2.34].

Finally, it is possible to limit the amplitude by using clipping devices, e.g. diodes. This method usually leads to noisy oscillators and is rarely used in high-performance RF VCOs.

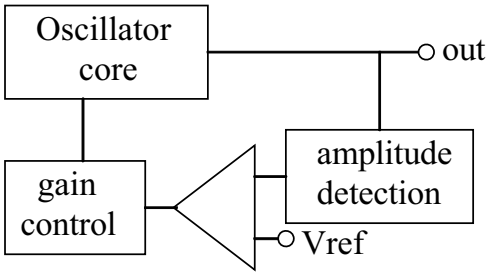


Figure 2.5. Automatic amplitude control loop.

2.2 Van der Pol Oscillator

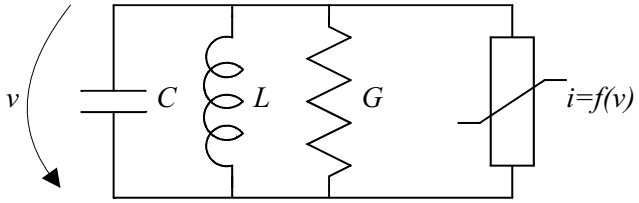


Figure 2.6. Van der Pol oscillator.

The simplest LC oscillator is depicted in Figure 2.6. It consists of a single LC resonator with a loss conductor G and a nonlinear negative conductance element. As it is the simplest possible structure, it will be used here for studying various oscillator properties. Let us first consider a case where the negative conductor follows

$$i = f(v) = -g_1 v + g_3 v^3 \qquad g_{1,3} > 0 \tag{2.5}$$

and large-signal (or dynamic) conductance $G_{LS} = \dfrac{di}{dv} = -g_1 + 3g_3 v^2$ (2.6)

The small-signal conductance is $-g_1$, and consequently, the circuit starts to oscillate if g_1>G. The slope of *f(v)* remains negative until *df/dv*=0, and the sum of the conductances remains negative in the region limited by V_{NC}. This is symbolically expressed as

$$G + G_{LS}(v) = 0 \tag{2.7}$$

$$\Rightarrow \quad V_{NC} = \sqrt{(g_1 - G)/3g_3} \tag{2.8}$$

Thus, with amplitudes smaller than this value the LC resonator absorbs energy, and with larger amplitudes it dissipates energy. For physical reasons, it is assumed that oscillation will stabilize with a balance of dissipation and absorption. Hence, it is assumed that an oscillation will exist with an amplitude somewhat larger than the previously calculated V_{NC} and the oscillation frequency is that defined by the resonance frequency of the LC resonator.

The balance of energy requires

$$\int_0^T v(t)\cdot i(t)\,dt = 0 \tag{2.9}$$

Assuming sinusoidal oscillation with an angular frequency of one, we have $v = A\cdot\sin t$ and, by substituting this into Eq. 2.5 and thereafter into Eq. 2.9, we get

$$\int_0^{2\pi} A\sin t\left[(G-g_1)A\sin t + g_3A^3\sin^3 t\right]dt = 0 \tag{2.10}$$

By solving this equation, an estimation for the oscillation amplitude is

$$A = \sqrt{\frac{4}{3}\frac{g_1-G}{g_3}} = 2V_{NC} \tag{2.11}$$

Note that an idea that occasionally appears in the literature, that $G+G_{LS}(v)=0$ (Eq. 2.7) would define the oscillation amplitude leads to an incorrect result (V_{NC}). Alternatively, one might consider that the oscillation amplitude is found from $G+G_{AVE}(v_{osc})=0$, where the average negative conductance G_{AVE} is defined by the interception points of the line $i=G_{AVE}\cdot v$ and the f(v) curve. This also leads to an incorrect result ($\sqrt{3}V_{NC}$). Equally, a wrong result is achieved if we consider that the average negative conductance balances the losses. In such a case we have

$$G + \int_0^T G_{LS}(v)\,dt = 0 \quad\Rightarrow\quad A = \sqrt{2}V_{NC} \tag{2.12}$$

Using Kirchoff's current law for more detailed analysis, the circuit is described by

$$\int\frac{1}{L}v\,dt + C\frac{dv}{dt} + vG + f(v) = 0 \tag{2.13}$$

After the substitution of *f(v)* and differentiation, we have

$$LC\frac{d^2v}{dt} + L(G-g_1+3g_3v^2)\frac{dv}{dt} + v = 0 \tag{2.14}$$

With the introduction of time normalization ($\tau = t/\sqrt{LC}$), voltage normalization ($v=h\cdot u$), and the van der Pol parameter $\varepsilon = (g_1-G)\sqrt{\frac{L}{C}}$, the van der Pol equation takes a general form

$$\frac{d^2u}{d\tau} + \varepsilon(u^2-1)\frac{du}{d\tau} + u = 0 \tag{2.15}$$

The magnitude of ε determines the closeness of the circuit to the ideal harmonic resonator. If ε=0, this reduces Eq. 2.15 to the DE of a harmonic resonator. This observation justifies the earlier analysis on the oscillation amplitude for cases where ε is very small. The characteristic roots of the corresponding linearized system $p^2 - \varepsilon p + 1 = 0$ (2.16)

are $$\lambda_{1,2} = \frac{1}{2}\cdot(\varepsilon \pm \sqrt{\varepsilon^2-4}) \tag{2.17}$$

Clearly, a boundary exists at ε=2, and ε>2 has been proposed as a definition for relaxation oscillation [2.35]. The importance of Eq. 2.15 is that it reveals that solely ε defines the characteristics of the oscillator. In particular, the nonlinear coefficient g_3 simply scales the oscillation amplitude, and it does not have any other impact.

B. van der Pol initially studied this case in the 1920s, and since then mathematicians have used it extensively in the study of differential equations. In his paper [2.36], van der Pol derives an approximate solution for Eq. 2.15 and, using the symbols we adopted previously, the result is

$$v(t) \approx \sqrt{\frac{4}{3}\frac{g_1 - G}{g_3}} \cdot \cos\left(\frac{1}{\sqrt{LC}}t\right) \frac{1}{\sqrt{1 + e^{-\omega_0 \varepsilon (t - t_0)}}} \tag{2.18}$$

Thus, the oscillation amplitude is the same as was previously achieved with the power integral, the oscillation frequency is that of the natural frequency of the LC resonator and the amplitude growth is dependent on ε.

As already stated, if ε<<1 the VDP oscillator resembles a harmonic resonator, and approximate analytical analysis is possible. The opposite extreme, a very large value for ε, enables us equally to use simplifications for analyzing the behavior of the circuit. In such a case the circuit operates in relaxation mode. We will substitute ε for μ to emphasize that μ>>1, and rewrite Eq. 2.15 as

$$\mu(u^2 - 1)\frac{du}{d\tau} = -\frac{d^2u}{d\tau} - u \tag{2.19}$$

Here μ is large and u is bounded to a fairly small value. Hence, either $du/d\tau$ is small or the left hand side is large. In the latter case, $d^2u/d\tau$ has to be large, since u is not. In a crude manner this argumentation suggests that either the motion is very slow (the left-hand side is small and balanced by -u) or the motion is rapid. Figure 2.8 depicts this kind of relaxation oscillation in a VDP oscillator. We can observe that the waveform consists of an exponentially increasing (or decreasing) part and a "relaxing" part. With some amount of mathematical manipulation it can be shown that the normalized oscillation frequency for relaxation oscillation is roughly $\omega = 3.9/\mu$ [2.6],[2.36]. Indeed, as soon as we increase the nonlinearity of the oscillator (ε increases) the oscillation frequency is shifted from the resonance frequency of the LC resonator. Buonomo's derivation [2.37] for the normalized oscillation frequency is

$$\omega(\varepsilon) = 1 - \frac{1}{16}\frac{\varepsilon^2}{1+\varepsilon^2} - \frac{175}{3072}\frac{\varepsilon^4}{(1+\varepsilon^2)^2} - \frac{45469}{884736}\frac{\varepsilon^6}{(1+\varepsilon^2)^3} - \cdots \tag{2.20}$$

For instance, ω(0)=1, ω(0.4)=0.990 and ω(1)=0.948. More than the above three terms are required for larger values of ε.

Now we know that in the presence of nonlinearity the oscillation frequency is shifted from the LC resonance frequency. Considering our primary mission here, gaining a general understanding of the oscillation phenomena, the actual question is why this frequency shift takes place. This question was resolved by Groszkowski [2.38],[2.39] and the approach is called the method of reactive power balance of harmonics. It is based on the relationship between the voltages and currents in the nonlinear negative conductance on one hand, and the same quantities in the resonant circuit on the other. The shape of the voltage and current in both elements must be identical and the two relationships, one for the active circuit and the other for the passive, must coexist. This means that the oscillation frequency must shift until

both relationships are mutually met. Mathematical analysis of this issue [2.39] leads to the following relationship, where y_n is the admittance value at the n^{th} harmonic.

$$im\{y_1\} = -\sum_{n=2}^{\infty} n \frac{V_n^2}{V_1^2} im\{y_n\} \tag{2.21}$$

At the LC resonance $im\{y_1\}=0$, whereas here we can observe that in the presence of harmonic content a frequency shift must occur to satisfy the above relation. The frequency shift is interrelated with the amount of harmonic generation and reactive admittance seen at each harmonic. The frequency shift is minimized by attenuating the harmonics, i.e. using a high-Q resonator. The result also reveals the possibility of oscillator synchronization at a higher harmonic.

Finally, considering the basic VDP oscillator, we may express the LC resonator impedance as

$$im\{y_n\} = n\omega C - \frac{1}{n\omega L} = \frac{1}{n\omega L}(n^2 \frac{\omega^2}{\omega_{res}^2} - 1), \quad where\ \omega_{res}^2 = \frac{1}{LC} \tag{2.22}$$

With the aid of Eq. 2.21 the frequency shift can be expressed as

$$\frac{\omega^2}{\omega_{res}^2} = \frac{\sum_{n=1}^{\infty} V_n^2}{\sum_{n=1}^{\infty} n^2 V_n^2} \tag{2.23}$$

Thus, the oscillation frequency becomes smaller with increased nonlinear behavior. Incidentally, van der Pol derived the same result using an alternative method in [2.36].

2.2.1 Numerical Analysis of the van der Pol Oscillator

The characteristics of the van der Pol oscillator are demonstrated in this section by varying the VDP parameter ε. The van der Pol oscillator in Figure 2.6 has the following parameters:

1.	Excess gain	$GX=g_1/G$
2.	Characteristic impedance of the LC resonator:	$Z_0 = \sqrt{L/C}$
3.	Quality factor of the LC resonator:	$Q = 1/(\omega_{res} LG)$
	where	$\omega_{res} = \sqrt{1/LC}$
	and the VPD parameter can now be expressed	$\varepsilon = (GX-1)/Q$

(2.24)

In a mathematical context the VDP equation is studied by varying ε. However, from the electrical engineering point of view, it actually includes two cases: the variation in the excess gain and the variation in the quality factor. The excess gain is of special interest, since it is the parameter, which is freely selected by the designer. Some amount of excess gain is required for a safety margin in real circuit design, and the oscillation amplitude is also affected. In terms of the parameters that are introduced, the analytical solution for the oscillation amplitude can be expressed as

$$A = \sqrt{\frac{4}{3}\frac{1}{g_3} \cdot \frac{GX-1}{Q \cdot Z_0}} = \sqrt{\frac{4}{3 \cdot g_3} \cdot \frac{1}{Z_0} \cdot \varepsilon} \tag{2.25}$$

Prior to numerical results in tabulated form, it is illustrative to look at various oscillation modes as depicted in Figures 2.7-2.9. In general, the nonlinearity of the oscillator is controlled by ε, and here we keep the quality factor constant (Q=10) and alter the excess gain GX. As g_3 does not have an influence on ε it can be used as a scaling parameter for the amplitude. The three cases depicted in the figures have scaling $g_3 \rightarrow g_3 \cdot (GX-1)$.

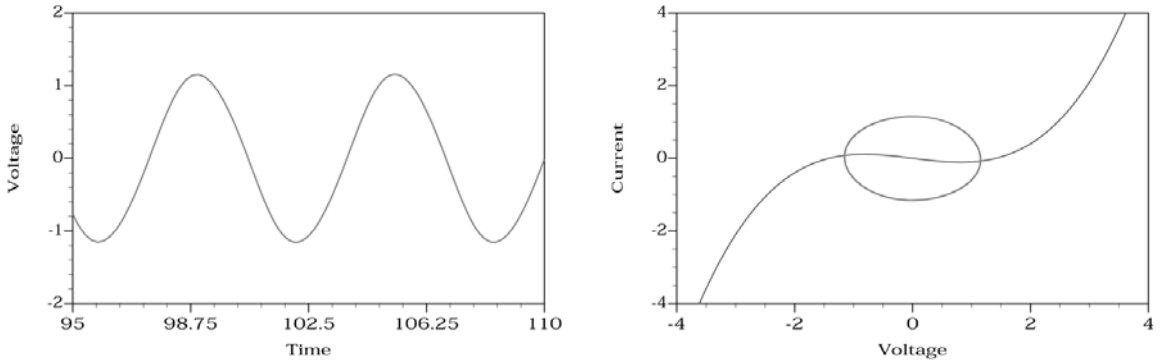


Figure 2.7. Sinusoidal oscillation: **ε=0.1**, GX=2, and Q=10. On the right, *f(v)* is also depicted.

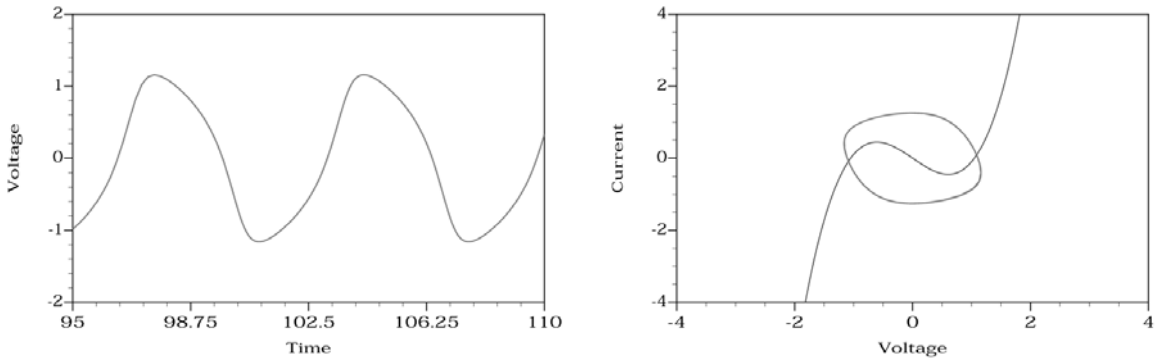


Figure 2.8. Distorted sinusoidal oscillation: **ε=1**, GX=11, and Q=10.

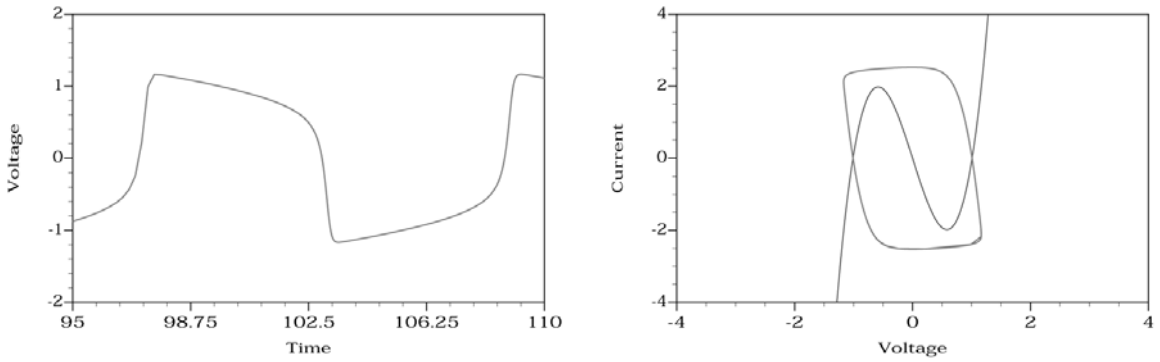


Figure 2.9. Case 3: relaxation oscillation: **ε=5**, GX=51, and Q=10. Here we can observe that the waveform consists of an exponentially increasing (or decreasing) part and a "relaxing" part.

The simulation results presented in Table 2.1 confirm Eq. 2.23. As soon as we introduce any excess gain, the oscillation frequency ω_{osc} is shifted downwards from the resonant frequency ω_{res}. Since all reactive elements are linear, this phenomenon is purely a property of the nonlinear behavior itself. More detailed simulation results of the frequency shift are depicted in Figure 2.10. Note from Table 2.1 that the simulated voltage swing and the one calculated with Eq. 2.25 are almost equal. The simulations also confirm that the variation of Z_0 or g_3 does not

have any influence on the oscillator characteristics. By sweeping Q and GX in such a manner that ε remains constant, one can ensure that the oscillator behavior is indeed solely controlled by ε.

Table 2.1. VDP oscillator characteristics as excess gain GX is swept. (Q=10, g_3=0.1)

GX	ε	$\omega_{osc}/\omega_{res}$	V_{osc}	THD_{20} [%]	V_{osc}/A
1.1	0.01	1.00	0.12	0.13	1.00
2	0.1	0.999	0.37	1.3	1.00
3	0.2	0.998	0.52	2.5	1.00
4	0.3	0.994	0.63	3.7	1.00
5	0.4	0.990	0.73	5.0	1.00
10	0.9	0.953	1.1	11	1.01
20	1.9	0.836	1.6	21	1.02
30	2.9	0.720	2.0	27	1.04
40	3.9	0.624	2.4	31	1.05
50	4.9	0.548	2.7	34	1.05

In Table 2.1 Eq. 2.25 defines the amplitude A and the harmonic distortion is given by

$$THD_n = \sqrt{\frac{\sum_{k=2}^{n} V_k^2}{V_1^2}} \tag{2.26}$$

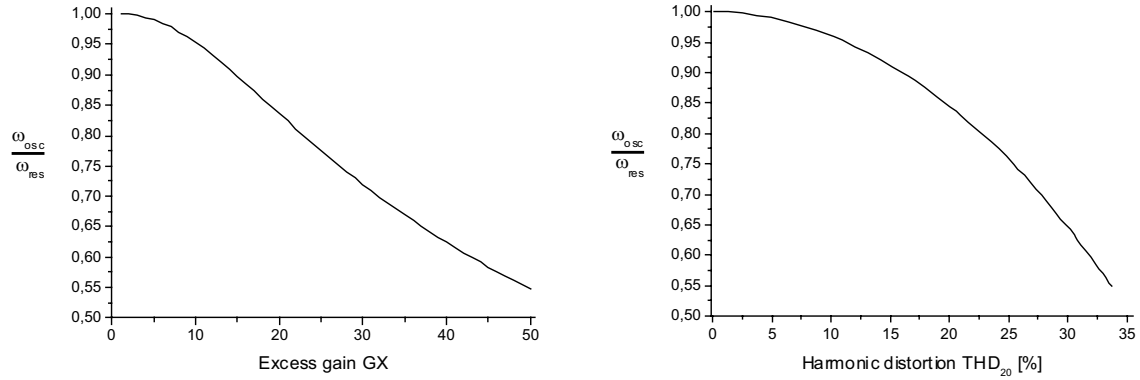


Figure 2.10. Frequency shift as a function of excess gain and distortion in the VDP oscillator.

2.2.2 Nonlinear Capacitor in VDP Oscillator

Until now the only nonlinear element has been the negative conductor. Now we will study what effects are caused by a nonlinear capacitor in a large-signal oscillator circuit. One could repeat a somewhat similar study to the one here for a nonlinear inductor as well, but since such devices are rare and the analysis would correspond to this one, it is omitted.

As the very first comment, it is worthwhile to keep in mind that ideal reactive elements are lossless. Thus, a nonlinear capacitor too just stores energy; it does not dissipate any. Therefore, a nonlinear capacitor alone does not limit the oscillation cycle. When a large-signal oscillation signal takes place over a nonlinear capacitor, "averaging" occurs. Figure 2.11 illustrates a nonlinear capacitance curve and an oscillation swing over it to clarify this issue. We may

define two types of capacitances, namely effective capacitance C_{eff} and average capacitance C_{ave}:

$$\omega_{osc} = \sqrt{\frac{1}{LC_{eff}}} \Rightarrow C_{eff} = \frac{1}{L\omega_{osc}^2} \tag{2.27}$$

$$C_{ave}(V_{osc}, V_{bias}) = \frac{1}{2V_{osc}} \int_{-Vosc}^{Vosc} C(V_{osc}, V_{bias})\, dV_{osc} \tag{2.28}$$

Usually, these two are not equal and neither of them can be directly calculated from the small-signal capacitance. The effective capacitance C_{eff} includes the frequency transition caused by the nonlinearities (Groszkowski's principle). Thus, precisely speaking, the average capacitance C_{ave} is not the correct approach to analyzing nonlinear capacitors in an oscillator. However, if the distortion of the oscillation swing remains low, then these two are close to each other, and the intuitive idea that oscillation swing averages nonlinear capacitors is a useful concept. This capacitance averaging is actually quite an important issue in practical circuit design. First of all, significant discrepancies between the small-signal values and the averaged values do occur and therefore small-signal analysis fails to predict the proper oscillation frequency and tuning range. Furthermore, the VCO tuning gain K_{VCO} differs from that calculated using the small-signal values. Second, averaging binds together the oscillation amplitude and frequency. From the analysis point of view it leads to an iterative process: the oscillation amplitude affects the oscillation frequency, and a shift in frequency alters the amplitude. A detailed analysis of this matter can be performed by presenting voltages, currents, and an incremental time-dependent nonlinear capacitor c(t) with Fourier series. Such work is presented e.g. in [2.40]-[2.45].

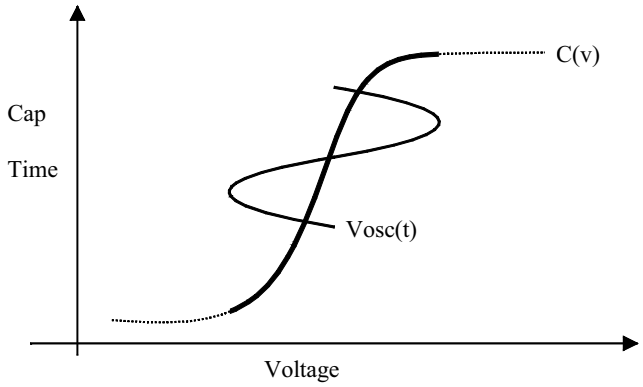


Figure 2.11. Nonlinear voltage-dependent capacitor C(v) and oscillation swing V_{osc} over it. The dark part of C(v) corresponds to the oscillation amplitude and represents c(t).

Tables 2.2 – 2.4 include simulation results with different types of capacitance nonlinearity. The VDP circuit itself is like before, with only the third-order nonlinearity and ε=0.2, GX=3, Q=10, and g_3=0.1. The first important observation is that the oscillation amplitude is strongly affected by C(v). So, instead of just negative conductance, or in general any active element, a nonlinear reactive element has an impact on oscillation limitation as well. However, a nonlinear lossless reactive element alone is not sufficient. Second, the oscillation frequency is shifted upwards and substantial distortion is generated with odd-order voltage dependency. One might wonder why a "linear" capacitor $C(v)=c_0+c_1v$ generates distortion. In capacitors the actual physical quantity is the charge. The linear capacitor $C(v)=c_0$ corresponds to $Q=c_0v$ and a voltage-dependent capacitor $C(v)=c_1v$ corresponds to a nonlinear dependency $Q=½c_1v^2$. The polynomial examples used here illustrate the situation well, but are not very physical. In real circuits reverse-biased pn-junction and MOS gate capacitances are the most important

nonlinear capacitors. Table 2.3 gives results from a VDP oscillator with a pn-junction type capacitor. The results reveal that this type of smooth C(v) has a fairly small impact on oscillator characteristics as long as we are far away from the built-in voltage ϕ. Note that C(v) becomes infinite at this voltage level, and a more detailed model is needed to simulate an oscillator in this region accurately. On the contrary, a highly nonlinear MOS capacitor generates high distortion in a similar manner to an odd-order polynomial capacitor. A nonlinear capacitor can shift the oscillation frequency in either direction, depending on its nature. Since it is also a significant source of distortion, it ruins the distortion – frequency shift relation found in the basic VDP oscillator. Therefore, oscillation signal distortion cannot be used as a simple design parameter, though it is usually a good idea to target for low distortion.

Table 2.2. VDP oscillator with a voltage-dependent capacitor $C(v)=c_0+c_1 \cdot v$, $c_0=1$.

c1	$\omega_{osc}/\omega_{res}$	V_{osc}	THD_{20} [%]
-0.5	1.04	1.30	30
-0.25	1.01	1.56	14
0	0.997	1.63	2.5
0.25	1.01	1.56	14
0.5	1.04	1.30	30

Table 2.3. VDP oscillator with a voltage-dependent capacitor $C(v) = C_0(1 - v/\phi)^{-1/2}$

ϕ [V]	$\omega_{osc}/\omega_{res}$	V_{osc}	THD_{20} [%]
20	0.997	1.63	2.8
10	0.997	1.63	3.7
5	0.994	1.63	5.9
2	0.989	1.61	9.4
1	0.911	1.40	33

Table 2.4. VDP oscillator with a voltage-dependent capacitor $C(v)=c_0+tanh(ST \cdot v)$, $c_0=1$.

ST	$\omega_{osc}/\omega_{res}$	V_{osc}	THD_{20} [%]
0	0.997	1.63	2.5
0.5	1.03	1.39	26
1	1.08	1.03	47
1.5	1.11	0.810	62
2	1.13	0.674	74

2.2.3 Small-Signal Stable Oscillator

As a curiosity, an interesting phenomenon can be observed by studying a VDP oscillator case where

$$i = f(v) = g_1 v - g_3 v^3 + g_5 v^5 \qquad g_{1,3,5} > 0 \tag{2.29}$$

Now the small-signal conductance is positive and according to the small-signal analysis this circuit is stable. However, the third-order term is negative and the large-signal conductance is

$$G_{LS} = g_1 - 3g_3 v^2 + 5g_5 v^4 \tag{2.30}$$

If the parameters are selected properly, a region exists where G_{LS} is negative.

Figure 2.12 depicts *f(v)* and the oscillation cycle. The polynomial coefficients $g_{1,3,5}$ were selected to be such that the figure is illustrative. Now, from the theoretical point of view, this example has an important message: a set of analog circuits does exists, which are stable in the small-signal analysis and yet are oscillators in reality. Small signal stability is not an adequate condition to ensure the stability of the circuit. From the point of view of the start-up conditions a pendulum clock is actually this type of oscillator. It is stable at rest and requires a sufficient perturbation for oscillation start-up. Note that this circuit was "kicked on" in a circuit simulator in a similar manner to all the previous cases, i.e., with an initial current on the inductor. In the real world, the start-up transients will make the job. As the quiescent point is a stable node, noise will not be a sufficient source of oscillation.

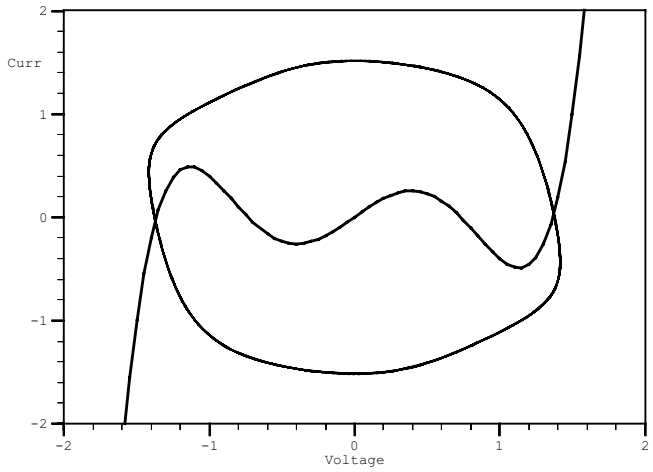


Figure 2.12. Oscillation in a small-signal stable VDP circuit.

2.3 Analysis and Simulation Methods

As an oscillator is a nonlinear autonomous circuit, oscillator analysis and simulation methods are not trivial matters, and a brief discussion is therefore worthwhile. In symbolic analysis we may distinguish linear and nonlinear methods. Linear analysis provides us with the initial conditions for the oscillation start-up. Although linear analysis methods yield exact results in the mathematical sense, it must be kept in mind that small-signal analysis is a coarse simplification of the actual large-signal oscillation. In practice we use linear analysis to find out the major contributors of oscillation frequency and excess gain.

Three commonly known methods for linear analysis exist. In the first method the circuit is divided into two parts, a generator circuit R_G+jX_G and a load circuit R_L+jX_L. Oscillation start-up occurs if

$$\begin{aligned} X_G(\omega_0) + X_L(\omega_0) &= 0 \\ R_G(\omega_0) + R_L(\omega_0) &< 0 \end{aligned} \tag{2.31}$$

In the second method the oscillator is considered as an unstable feedback system. It consists of an amplifying section A(s) and a frequency-selective feedback network B(s). The transfer function of the system is given by

$$H(s) = \frac{A(s)}{1 - A(s)B(s)} \tag{2.32}$$

The circuit is unstable when the open-loop gain A(s)B(s)=1. Thus, in feedback system analysis the circuit is unstable when the total phase shift is 360° and the gain is greater than unity.

In the third method the oscillator circuit is represented using nodal equations. The determinant of the system must be equal to zero for nontrivial solutions. This is expressed by

$$[Y]\cdot[V]=0 \quad \Rightarrow \quad |Y|=0 \tag{2.33}$$

The selection of the preferred method depends on the oscillator topology and corresponding design philosophy. There are some practical, as well as theoretical, problems in these methods. In the negative resistance analysis there is no way to decide how to divide the circuit into two segments [2.46], and in a similar fashion in the loop-gain method it is not unambiguous how to define A(s) and B(s). In the nodal equation method only two rows and columns of the deterministic determinant are used, and extra rows and columns, i.e. additional nodes in the circuit, must be neglected. See at [2.47] for more details. Precisely speaking, none of the above methods guarantee that the circuit is an oscillator and more detailed analysis is needed if we want to be precise. An extended and more sophisticated version of the negative resistance analysis is known as Kurokawa's method [2.48]. It provides better results for finding out if the circuit and bias point under study are truly unstable. Equally, in the loop-gain method we may use the Nyquist diagram for more detailed stability analysis [2.49].

In the van der Pol oscillator context we have already discussed nonlinear symbolic analysis. Generally, it is not possible to find exact solutions, but in some cases we may use quasi-sinusoidal oscillation approximation, and derive a result. Something that is close to this approach is the use of describing functions; see e.g. [2.4], [2.50]. Alternatively, in some cases the oscillation current flows only for a fraction of the cycle, and during this time its value can be approximated to be constant. Thus, large-signal analysis is carried out by defining a square wave current with an amplitude and conduction angle.

Since symbolic analysis methods are limited to highly simplified cases, computer-aided numerical methods play an essential role in the oscillator design. Oscillators are more sensitive to simulator errors than most other circuits. They are also somewhat out of the mainstream, and as they are peculiar circuits with special needs the simulation methods are not as well established as for more common circuits. Luckily, the RF IC boom has provided remedies with respect to this issue. Still, in practical circuit design one may notice that different simulators or simulation methods give discrepant results. This brings an inconvenient uncertainty to oscillator design, and thus motivates the circuit designer to pay attention to simulation issues. Note that these discrepancies may be caused by tools or by device models.

Small-signal (AC or S-parameter) analysis can be used to check the initial instability and sufficient excess gain. Its validity is limited, as already discussed. Transient analysis – the traditional time-domain simulation method is mature and applicable to all circuits. In oscillator simulations one must ensure that the simulator is able to capture the possible oscillations. Most transient simulators fail to predict oscillations with standard settings. The following procedure is needed:

1) ensure proper start-up conditions by defining some time-domain variation for the DC operation point. This can be done by setting the initial current for the inductor or the initial voltage for the capacitor, by applying a "no prior DC analysis" setting, or by letting the supply voltage increase slowly towards the final value.
2) avoid an excessive analysis time-step by defining a constant time-step, which should be about one tenth of the expected oscillation cycle.
3) increase the accuracy definitions. High-Q resonators tend to store and accumulate numerical errors resulting in a slight error in the period of oscillation. Tight accuracy settings and small time step reduce this effect. The trapezoidal rule is a good choice for the numerical algorithm [2.51].

Transient simulations have some fundamental problems. As a result of the above necessary settings the simulations are time consuming and the results are not readily available in an easily observed form. Furthermore, time-domain noise analysis is not a practical method for oscillator phase noise analysis. Devices defined only in the frequency domain, such as transmission lines and user-defined elements like frequency-dependent resistors, pose a challenge for the simulator, and though modern simulators are capable of dealing with these devices in most cases, this is still a problem.

As an alternative to transient simulation, a periodic steady state can be sought either in the time domain using the shooting method [2.52] or in the frequency domain using the harmonic balance method [2.53]. In addition to these, other less popular methods exist, as well as many modifications of these two basic methods. The details of these lie beyond the scope of this discussion. General discussion of these matters can be found in [2.54]-[2.56]. From the oscillator design point of view the main benefit of the steady-state methods is that the final result can be subjected to small fluctuations, i.e., noise, and thus phase noise analysis can be performed [2.57].

During the 1990s SPICE-type simulators did not include frequency domain methods, and they were found only in microwave engineering-oriented tools. *Hewlett-Packard's Microwave Design System (HP MDS)* was one of the market leaders, and that was the one I used. The reliability of these tools was not very good, and anomalies were often found in the simulation results. Along with the RF IC boom, the IC CAD tool market leaders *Cadence* and *Mentor* implemented steady-state analysis tools into their SPICE-type products. For instance, nowadays *Mentor's Eldo RF* is able to analyze operation and phase noise not only in oscillators, but also in them when they are combined with frequency dividers and mixers. For this tool, I have rarely observed any anomalies in recent releases and the results seem reliable, and are in good agreement with measurements.

For the harmonic balance method it is not as easy as for the transient analysis to give simple guidelines for proper use. The exact algorithm implementation and nomenclature vary in different tools. Signals are represented with Fourier series in these simulations and the optimization procedure is used for finding the result. This means that the simulator is not able to find signals other than the found fundamental and its overtones. Multi-oscillations, chaotic behavior, or low-frequency ringing (squegging) are not found. Either the existence of these problems appears by convergence failure, or they are simply not found. The calculation algorithm in these tools includes time-to-frequency (and vice versa) conversion using the Fourier transform. The FFT over-sampling factor should be set to at least a value of three in order to avoid aliasing and to increase accuracy. Furthermore, an appropriate number of harmonics should be selected. For typical RF IC VCO cases ten is a good value. Sometimes the analysis method includes a short initial time-domain analysis, and for these cases one must adopt the previously mentioned time-domain guidelines.

To conclude this discussion, I would say that the reliability of oscillator simulations was still doubtful in 1990s, but nowadays this problem is mostly obsolete, and the simulation results are, generally speaking, correct, assuming that the end-user knows what he or she is doing.

2.4 Phase Noise

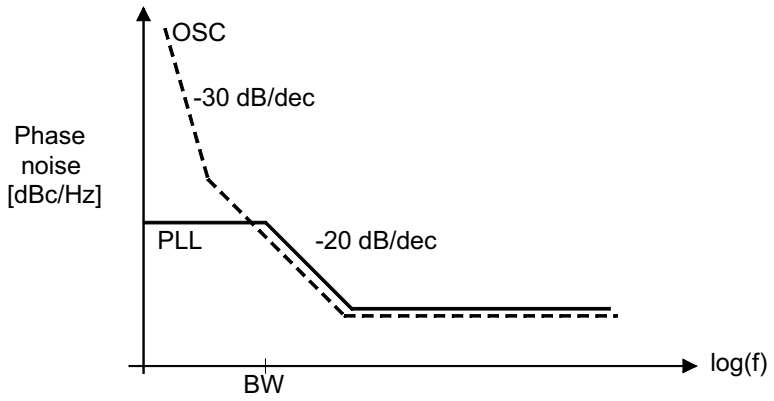


Figure 2.13. The phase noise of a free-running oscillator is shown with a dashed line and the noise of the complete PLL is shown with a continuous line. Outside the PLL loop bandwidth (BW), the oscillator noise dominates and it is slightly increased by the PLL locking.

In practical oscillator design and in circuit development the oscillator phase noise plays a particular role. It is often the limiting performance metric, and thus requires special attention. Most of the performance metrics, such as the tuning range, power consumption, or die area, are conceptually simple, whereas phase noise is an intricate matter. This section discusses general topics associated with phase noise, its impact on radio systems, and theories related to it. Circuit-oriented phase noise issues are dealt with in conjunction with the actual oscillators.

Consider an oscillator with a stable orbit, such as the one depicted in Figure 2.7. Now we will disturb this trajectory by applying a small impulse. The trajectory is perturbed but because the oscillator is a stable system it will eventually return to the original orbit. Thus, we can represent the sinusoidal but disturbed output voltage of the oscillator by

$$v(t) = (A + \alpha(t)) \cdot \cos(\omega_{osc} t + \phi(t)) \tag{2.34}$$

The amplitude deviation $\alpha(t)$ will decay as a result of the internal tendency of oscillators to settle into a stable orbit. In an autonomous oscillator there is no specific time reference. Therefore, any disturbance in the phase simply shifts the oscillation, and it continues as if it had never been disturbed. There is no internal mechanism for decaying phase disturbances, and therefore phase deviations accumulate. These deviations caused by noise sources are called phase noise. Phase noise spreads oscillation energy to a larger bandwidth. This phenomenon can also be considered as a phase diffusion process [2.58]. Phase noise has a Lorentzian spectrum and appears as noise sidebands in the spectrum of the oscillator as sketched in Figure 2.13 in log scale and in Figure 2.14 in linear scale. The width of the Lorentzian plateau is called the oscillator line width and it is so narrow in ordinary oscillators that it is not visible in conventional RF measurements. 1/f noise dominates the spectrum close to the carrier, and phase noise drops by 30 dB per decade. At larger offsets, where thermal noise dominates, the drop is 20 dB/dec, and finally the actual phase noise spectrum falls below the noise floor and the observed spectrum is flat at high offsets. In typical radio transceivers a free-running oscillator is coupled to a highly stable reference with a phase-locked loop (PLL). Such an arrangement results in phase noise being attenuated inside the PLL bandwidth. Other components of the PLL contribute to the noise level inside the PLL bandwidth and in a simplified analysis the noise level inside the PLL bandwidth is flat. Phase noise spectra for free-running and locked oscillators are depicted in Figure 2.13. The phase noise is quantified

with single-sided noise density in units of decibels-to-carrier per hertz, and is denoted by the symbol $\mathcal{L}$, or the acronym N/C. It is given to respect with an offset frequency f_m.

$$\mathcal{L}(f_m) = 10\log\frac{noise\ power\ at\ frequency\ f_{osc}+f_m}{carrier\ power\ at\ f_{osc}}\left[dBc/Hz\right] \tag{2.35}$$

2.4.1 Phase Noise in Radio Systems

In telecommunication systems the phase noise of an LO signal is of great concern since it impairs the quality of the reception. Consider the case shown in Figure 2.14a. We have a weak signal with a strong signal in the adjacent channel. The phase noise of the LO signal falls on top of these signals in down-conversion, and results in the strong "interferer" signal overwhelming the weak signal. This phenomenon is known as reciprocal mixing. Impacting parameters, such as the channel spacing, accepted signal strengths, and signal-to-noise ratio (SNR), or carrier-to-interference ratio (C/I), are given in telecommunication system specifications. The phase noise requirement can be calculated using dB-values from

$$\mathcal{L}(f_m) \ < \ S_{sig} - S_{block}(f_m) - 10\log(BW_{channel}) - SNR \tag{2.36}$$

For instance, in the second-generation cellular system GSM the lowest signal strength S_{sig}= −102 dBm, interferer S_{block}(600 kHz)=-43 dBm, channel bandwidth $BW_{channel}$=200 kHz, and the required SNR=9 dB. This gives us a phase noise specification $\mathcal{L}$(600 kHz)<-121 dBc/Hz, and then a margin of 5-10 dB should be added to establish a practical target.

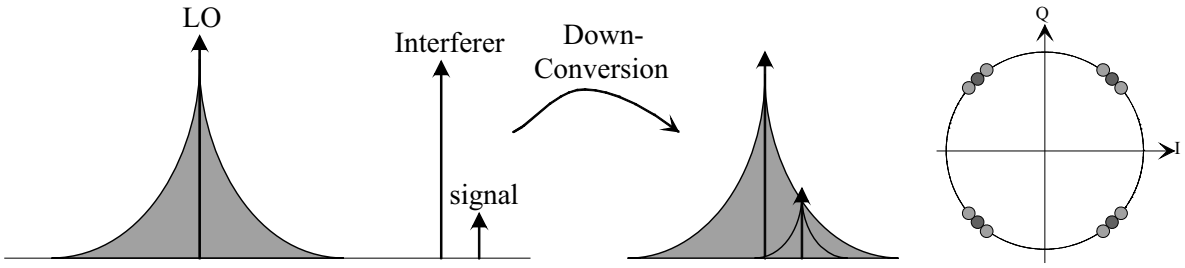


Figure 2.14. (a) Reciprocal mixing: the strong interference signal corrupts the reception under the influence of a noisy LO signal. (b) The IQ constellation (here QPSK) scatters as a result of noisy LO [2.59].

Reciprocal mixing is the limiting factor for acceptable phase noise in conventional narrowband systems, and the issue is well understood. The estimation of a sufficient phase noise level is more challenging in modern digital communication systems utilizing advanced coding techniques. For instance, orthogonal frequency division multiplexing (OFDM) is a popular choice for wideband communication systems because of its robustness in a hostile multi-path environment. In OFDM systems the data stream is divided into multiple low-rate streams, and each is modulated with a sub-carrier. The actual OFDM signal consists of multiple spectrally orthogonal sub-carriers. A comprehensive explanation can be found in, for example, [2.60]. Signal bandwidths in typical OFDM systems are large (e.g. 22 MHz in WLAN), and hence reciprocal mixing is not an issue. Phase noise causes two distinct effects for the sub-carriers. Common phase error (CPE) causes sub-carrier phase rotation. Intercarrier interference (ICI) introduces interference to a sub-carrier from all the other sub-carriers. It breaks down the orthogonality between the sub-carriers. An early paper [2.61] on phase noise in OFDM systems considered only cases with free-running oscillators, and though authors were able to provide an

analytical relationship, its validity is questionable. In [2.62] the PLL noise is integrated and re-converted into free-running oscillator line width so as to be able to use the result of [2.61]. In a recent paper [2.63], a real PLL noise model is used, but no final analytical relationship is given. This is caused by two facts. First, both CPE and ICI can be compensated for with special algorithms in the digital domain [2.64]-[2.65], and this compensation process is not linear. In other words, the effect of the correlation algorithm depends on the phase noise level. Second, the sensitivity of a system to phase noise and the performance of phase-noise suppression algorithms do not depend only on the transmission system itself, but also on the type of channel [2.63]. Therefore, in practice the impact of phase noise in an OFDM system is analyzed in a system simulator. Such a phase noise simulation example for a multi-band OFDM ultra-wideband (MB-OFDM UWB) receiver is shown in [2.66]. Generally, the accepted phase noise level for OFDM systems is defined in terms of total integrated phase noise, and integration is performed over half of the bandwidth [2.67].

Finally, I have collected a list of phase noise requirements for various systems from the open literature, given in Table 2.5. In the last column a normalized phase noise value is given. It shows that there is a 40-dB difference in the requirements, and narrowband systems and satellite communication are the most challenging of the selected cases.

Table 2.5. Phase noise requirements for some telecommunication systems.

System	Band [MHz]	Channel spacing [kHz]	Phase noise [dBc/Hz]@kHz	Norm-N/C[1] [dBc/Hz]
IS54	824-894	30	-115@60	-132
GSM	890-960	200	-121@600	-120
DECT	1880-1900	1728	-97@1800	-91
UMTS	1920-1980	5000	-129@8000	-111
WLAN (b)	2400-2483.5	22000	-103@1000	-105
BlueTooth	2400-2483.5	1000	-109@1000	-111
GPS	1575.42	-	-95@1000	-93
DOCSIS	47-862	6000	-82@10	-100
DVB-S	10700-12750	fixed LO1	-95@100	-131
UWB	3432-10560	528000	-90@1000	-97

[1] Phase noise normalized to f_{osc}=2 GHz and offset f_m=1 MHz, N/C~$(f_{osc}/f_m)^2$

2.4.2 Phase Noise Theories

Phase noise has been under research for many decades, and many theories have been proposed. One of the first papers focusing on noise in oscillators in modern terms was a paper by Edson in 1960 [2.68]. An early milestone was a special issue on frequency stability of Proc. IEEE, Feb. 1966. This issue included, among others, a paper by Hafner [2.69], which proposed the idea of studying the response of an oscillator to an impulse, and perhaps the most cited paper in the oscillator literature, the Leeson's model [2.70]. In his book published as late as 1982 [2.71], Robins claims that he also derived a similar expression to Leeson in 1964 but did not publish it. Generally we can say that during the 1960s quasilinear, or linear time-invariant (LTI) as they are often called nowadays, analysis methods for oscillator phase noise were established. In 1969 Kurokawa proposed a method for analyzing the stability of the operating point of an oscillator [2.48]. Kurokawa's method was a popular one among microwave engineers, but it has not withstood the test of time, and is nowadays rarely seen in use among RF IC designers. Nevertheless, Kurokawa was among the pioneers trying to figure out the impact of the nonlinear nature of oscillators. Kaertner's work in 1990 [2.72] was quite seminal since it made no assumption about the type of oscillator or its non-linearity. In the method an oscillator is

described with a set of differential equations and the solution is then slightly perturbed for noise analysis. The result of these differential equations can also be considered with the oscillator trajectory (limit cycle) and how this is perturbed under the influence of noise. Demir's work [2.73]-[2.74] resembles and extends Kaertner's work, and to my knowledge, his work is the most rigorous and general phase noise analysis published in the open literature. However, at the same time it is mathematically intricate, not at all intuitive, and does not provide analytical guidelines for the circuit designer. Instead, Demir's work is well suited for computer simulations, and both Kaertner and Demir actually emphasize this in their text. Hajimiri and Lee developed a phase noise theory based on the impulse sensitivity function (ISF) of an oscillator [2.75]. The method is able to provide some insight into topological questions, and therefore we will return to it soon. Huang [2.76] analyses oscillators in the time domain, and also derives analytical solutions for phase noise by considering how the noise modulates the oscillator. Abidi's group follows the same approach [2.77],[2.44]. What is common to both of these works is that they are targeted towards explicit circuit-parameter-related closed-form solutions. Huang deals with the Colpitts oscillator, and Abidi's group with the cross-coupled MOSFET pair. It is clear that their work is restricted to the selected circuit, but the same approach can be used for other oscillators as well. When debating the accuracy of each phase noise theory, it is imperative to understand that they are focused on different purposes. The aforementioned works cover rigorous theoretical work suitable for numerical analysis, methods for topological analysis, and a circuit design-related approach with analytical formulas. From the strictly theoretical point of view, some of these do not withstand scrutiny, and yet they are useful in practical engineering and have led the art of oscillator design forward.

Next, we will have a closer look at the linear noise model and the ISF model. Prior to that, it will be illuminating to consider two simple models or ways of thinking:

VCO / ICO model: any real electrical oscillator includes a nonlinear device. This device has a nonlinear voltage-current relationship, and it includes a parasitic voltage-dependent capacitance. Therefore, we may consider that any real oscillator is conceptually a voltage-controlled oscillator and/or a current-controlled oscillator. Any fluctuation in any nodes of the oscillator will slightly disturb the oscillation. Thus, noise is modulating oscillation frequency, which appears as phase noise.

Mixer model: in the second model we consider the oscillator as a nonlinear element, and consequently it is a mixer. Now we may consider noise as one input signal for the mixer, and the oscillation signal itself as the second input. In the output we observe noise induced sidebands as a result of the mixing phenomenon.

To establish a linear noise model we can once again consider the VDP oscillator, and there we have a noise source related to the loss conductance in parallel with the resonator. The resonator impedance is

$$Z(\omega_0+\omega_m) = -j\frac{(\omega_0+\omega_m)L}{1-(\omega_0+\omega_m)^2 LC} \tag{2.37}$$

When the definitions in Eq. 2.24 for ω_0 and Q are used, and it is considered that $\omega_m << \omega_0$, the above simplifies to

$$\left|Z(\omega_0+\omega_m)\right| = \frac{\omega_0^2 L}{2\omega_m} = \frac{\omega_0}{2QG\omega_m} \tag{2.38}$$

Now the noise voltage is expressed as

$$\hat{v}_n^2 = \hat{i}_n^2 \left|Z\right|^2 = 4kTG\left(\frac{\omega_0}{2\omega_m GQ}\right)^2 = 4kTR\left(\frac{\omega_0}{2\omega_m Q}\right)^2 \tag{2.39}$$

This noise voltage includes both amplitude and phase components, which are equally distributed. Thus, only half is contributed to the phase noise. The carrier amplitude is given by $v_{sig}^2 = P_{sig} \cdot R$, and eventually the noise-to-carrier ratio is given by

$$N/C = \frac{\hat{v}_n^2}{v_{sig}^2} = \frac{1}{P_{sig}R} 2kTR\left(\frac{\omega_0}{2\omega_m Q}\right)^2 = \frac{2kT}{P_{sig}}\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \tag{2.40}$$

The famous Leeson model was derived for a feedback amplifier structure using a similar linear approach to the one above. Leeson's own text is somewhat brief, but Sauvage has presented a more detailed version of it [2.78]. The extended version of Leeson's model is expressed as

$$\mathcal{L}(f_m) = 10\log\left\{F\frac{2kT}{P_{sig}}\left[1+\left(\frac{f_0}{2Qf_m}\right)^2\right]\left(1+\frac{f_c}{f_m}\right)\right\} \tag{2.41}$$

Here we can see two additional parameters. F is an excess noise factor originally related to the additive noise of the active device. Nowadays we have to consider it as a fitting parameter including all the linear and nonlinear noise couplings. Parameter f_c describes the 1/f noise contribution. It is also a fitting parameter. Thus, Leeson's model must be seen as a representation of the measured phase noise spectrum. In general, there is no simple way to estimate F and f_c a priori. Furthermore, real oscillators follow this equation only partly. Increasing the oscillation power P_{sig} or quality factor Q a lot does not necessarily lead to a corresponding improvement in the phase noise. The term "1+…" is added to the model to describe the noise floor present in the measured results. However, an actual core oscillator does not really have such a phase noise floor, and the noise floor is due to the additive noise of devices in the oscillator itself, in the buffers, and in the measurement set-up. And yet, problematically, in Leeson's model the noise floor is directly bound to the oscillator parameters.

The impulse sensitivity function (ISF) model [2.75] considers the response of an oscillator to a charge impulse. If we inject a small charge impulse to an oscillator, we observe that

1) The charge to excess phase response is linear for small charges.
2) The response of the oscillator depends on the relative time instance at which the charge is injected.

On the basis of these two fundamental observations this model is categorized as linear time-variant (LTV) theory. The oscillator itself remains nonlinear considering its voltage-current relationship. The phase response of an oscillator is described by its time-variant impulse response

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{\max}} u(t-\tau) \tag{2.42}$$

where q_{max} is the maximum charge swing at the node and $u(\cdot)$ is the unit step. $\Gamma(\cdot)$ is called the impulse sensitivity function, and it is a dimensionless T-period frequency- and amplitude-independent function. It encodes information about the sensitivity of an oscillator to an impulse (and hence noise) injected at the relative phase point. Then, a superposition integral is used to calculate the total phase deviation at the output. The final step in the ISF model is to model the

phase-to-voltage transformation to obtain the output voltage waveform; see [2.75] for details. The phase noise resulting from one current noise source with white power spectral density is given by

$$\mathcal{L}(\omega_m) = 10\log\left\{\left(\frac{\Gamma_{rms}}{q_{\max}}\right)^2 \frac{\hat{i}_n^2}{2\omega_m^2}\right\} \tag{2.43}$$

All noise sources have to be inspected separately and then the results are summed to establish the complete phase noise spectrum. Thus, the use of the ISF technique as a practical design methodology is toilsome, particularly keeping in mind that in present-day simulation tools the noise contributions of the individual sources are readily available. Instead, the ISF model has been able to prove in a systematic and elegant manner some design guidelines known previously only as a result of design experiments or simulations. It provides a simple yet accurate way of dealing with cyclostationary noise sources. We simply replace Γ by $\Gamma_{eff}=\Gamma\cdot\alpha(t)$. Here $\alpha(t)$ is a periodic unitless function with a peak value of one, and a shape corresponding to the oscillation waveform. A cyclostationary noise source is described by $S(t)=S_{cons}\cdot\alpha(t)$. An example of a cyclostationary noise source is the channel noise of a transistor, which is dependent on the channel current and is therefore time-dependent. Considerations of the role of cyclostationary noise sources lead to the conclusion that in the best oscillator the active element delivers the required energy into the resonator all at once at that time point when the ISF has its minimum value [2.79]. Another major result of the ISF model is the insight gained for 1/f noise upconversion. The 1/f noise corner f_c of the phase noise spectrum is related to the 1/f noise corner $f_{c,dev}$ of the device by

$$f_c = f_{c,dev}\cdot\left(\frac{\Gamma_{dc}}{\Gamma_{rms}}\right)^2 \tag{2.44}$$

This formula directly proposes that with the reduction of Γ_{dc} the 1/f noise corner moves to a lower frequency. The reduction of Γ_{dc} is achieved either with a waveform with even symmetry about a point in the period or with a waveform with half-wave symmetry; that is, equal slopes of rising and falling edges [2.80]. In the original work of Hajimiri & Lee they propose three methods for calculating the ISF. They prefer using a numerical method, which is the most accurate but, at the same time, leaves us lacking the deeper insight often provided by analytical closed-form results. Andreani has made an impressive set of analyses for some common oscillator topologies using the ISF method, and he has derived closed-form formulas relating major noise sources to other design parameters; see e.g. [2.81]-[2.83].

LTI models give a discouraging view of oscillator design. Only physical parameters, such as the oscillation power or the quality factor of the resonator, matter. On the contrary, ISF theory clearly indicates that phase noise can be reduced by a proper choice of topology and device dimensioning, thus providing encouraging motivation for oscillator research.

2.4.3 Measurement Methods

RF measurement methods are a well-established piece of art. Once again, here oscillators, and particularly phase noise measurements are an exception. Since the measurement method impacts significantly on the phase noise result, it is worth discussing this matter briefly. The simplest and quickest phase noise measurement method is to use the spectrum analyzer directly. It is suitable for all oscillators regardless of the frequency or the power level. This method is, however, inaccurate. First, the drift of the oscillation frequency causes the result to deteriorate. Second, it does not distinguish between phase and amplitude noise. Third, the

phase noise of the analyzer's own local oscillator is added to the results. However, this is not a problem in the RFIC VCO measurements because of the poor phase noise characteristics compared to the analyzer's own LO, which has a high-Q resonator. Fourth, in some cases the dynamic range of the spectrum analyzer is insufficient. This problem is encountered in very high-frequency cases and a remedy is to down-convert the signal since spectrum analyzers have a better dynamic range at low frequencies.

The oscillation frequency of a free-running oscillator drifts back and forth. This is also called wandering or random walk. Wandering is due to low-frequency noise and environmental influence. Wandering results in close-in phase noise accumulating during the measurement sweep. This effect is illustrated in Figure 2.15. The constant curve is what we would like to measure, and the dashed lines represent the fluctuations of the signal. The problem is more severe near the carrier, while further away it is possible to achieve a reasonable result, although it will be a pessimistic one. Obviously, the faster the measurement is performed, the smaller the aliasing effect is. In addition, the resolution bandwidth (RBW) has to be low for accurate measurement, but the sweep time and RBW are inversely related. To demonstrate this, phase noise measurements with different sweep times are collected in Table 2.6, and the effect of RBW is shown in Table 2.7. The test device is a 2-GHz BJT LC-VCO [2.84] and the spectrum analyzer is a Rohde & Schwarz FSIQ40.

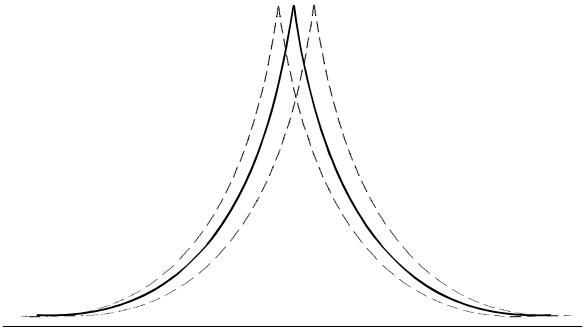


Figure 2.15. The oscillation frequency wanders during the measurement sweep. The actual result observed with a spectrum analyzer for each frequency slot is the accumulated power level.

Table 2.6. Phase noise vs. sweep time

Sweep time	$\mathcal{L}$(100kHz) [dBc/Hz]	$\mathcal{L}$(1 MHz) [dBc/Hz]
10 mS	-82.9	-103.6
20 mS	-80.9	-102.9
50 mS	-81.0	-103.0
100 mS	-80.2	-102.4
500 ms	-78.0	-100.9
1 s	-76.7	-99.8
5 s	-76.9	-99.6

Table 2.7. Phase noise vs. RBW

Resolution Bandwidth	$\mathcal{L}$ (100kHz) [dBc/Hz]	$\mathcal{L}$ (1 MHz) [dBc/Hz]
10 kHz	-80.1	-102.7
20 kHz	-81.0	-102.5
30 kHz	-80.2	-102.4
50 kHz	-71.5	-100.5
70 kHz	-70.4	-100.2
100 kHz	-57.3	-100.0

The problem of the oscillation frequency wandering can be circumvented either by following the wandering automatically, or by locking the oscillator to a clean reference. There are a large variety of arrangements reported in open literature. I intentionally do not provide a survey here. Just a brief glance at the most common methods is enough. The fundamental idea of the delay line method [2.85], which is also called the autocorrelation method, delay discriminator method, or frequency discriminator method, is to down-convert the signal with a replica of

itself delayed by a quarter of a period. The signal will be down-converted to DC and the noise sidebands can be measured directly at the respective offset frequencies. The delay line acts as a frequency discriminator for the offset frequencies $f_m << 1/\tau$. If the electrical delay is exactly ninety degrees, the amplitude noise is canceled. The system is tuned for maximum sensitivity to phase noise by varying the delay until a DC null is obtained at the IF output. If the phase shift is not precisely correct, the measured noise level is lower than in reality. A mathematical analysis of this method is presented in [2.86].

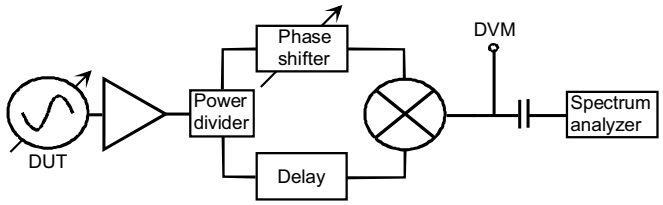


Figure 2.16. Delay line method.

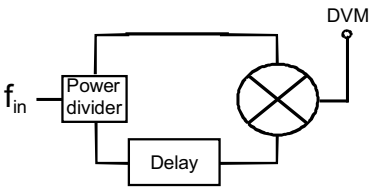


Figure 2.17. Measurement setup for the delay of a line.

Although the basic idea of the delay line method is relatively simple, there are some practical problems. An electrically tunable RF delay line is not a simple device. In a measurement lab an easier approach is to keep the delay line itself constant and put the required tunable phase shifter in the opposite path as shown in Figure 2.16. It is possible to achieve appropriate phase shift and proper power levels for both the LO and RF signals with this arrangement. At 2 GHz the wavelength is still about 15 cm and the available phase shifters can be tuned in length for about one centimeter, which means less than 20 degree phase tuning. Mechanical tuning is also very clumsy in practice. It is therefore easier to keep the phase shift constant (just a short cable) and tune the frequency of the DUT until an appropriate frequency is found. There is also a trade-off in the selection of the delay line. A long delay line ensures high sensitivity to phase noise but it may attenuate the signal too much and it will raise the noise floor. In practice, the delay line is a coaxial cable and therefore its length is limited to less than ten meters because of the attenuation and size. My delay line was a "recycled" ethernet cable. Its physical length is about six meters, its delay 37.8 ns, and its attenuation at 2 GHz is 11 dB. In Figure 2.17 a test setup for a delay line is shown. The input frequency is swept and the frequencies where the DC-nulls are achieved are observed. The delay is calculated from the interval of these frequencies.

$$\Delta f = f_1(DC=0) - f_2(DC=0) \qquad \tau = \frac{1}{2\Delta f} \tag{2.45}$$

A spectrum analyzer is used for the actual noise voltage V_{rms} measurement and the phase noise is calculated using the expression [2.87]

$$\mathcal{L}(f_m) = \frac{1}{2}\left(\frac{V_{rms}}{2\pi \mathrm{K}_\theta \tau f_m}\right)^2 \tag{2.46}$$

τ is the delay of the line and K_θ is the gain of the phase detector (mixer). Usually, the RF power level is quite low and therefore the mixer operating as a phase detector is not in a saturated mode. Hence, K_θ depends on the RF power level and frequency, and it has to be measured separately for each power level and frequency. The output of the phase detector has the shape of a saw tooth. Therefore, several measurement points have to be chosen and graphically checked in the measurement of K_θ. This method gives $\mathcal{L}$(100 kHz)=-91 dBc/Hz for the same VCO as was reported in Table 2.6. This result seems to be slightly optimistic indicating that exact quarter wave phase shift was not present.

Phase locking is a well-known method to synchronize a free-running oscillator to a clean reference. As already discussed (see Figure 2.13) the method increases the phase noise level at offsets beyond the PLL bandwidth. It is possible to build up a proper PLL set-up in a case-by-case manner. However, a general-purpose set-up is a difficult task since not only the oscillation frequency but also the VCO gain varies, and these have to be taken into account. Alternatively, injection locking [2.88] can be used to synchronize the oscillator-under-test to a clean reference oscillator. In the case of RF IC oscillators this method is quite difficult since RF IC oscillators are usually well isolated (typ. 40 dB) and it is therefore difficult to feed the injection signal.

Therefore, in the late 1990s I did some practically-oriented work based on these ideas with the aim of developing a low-cost general-purpose measurement set-up. It turned out to be relatively easy to build case-by-case type setups, but extending them to general-purpose use is difficult. Moreover, the accuracy of the measurements is always doubtful, particularly if the setup is altered. These practical considerations and work towards a versatile measurement setup became obsolete when a VCO/PLL tester (HP4352B) was purchased for our lab to support a particular PLL development project (not my work). The PLL tester gives $\mathcal{L}$(100 kHz)=-86 dBc/Hz and $\mathcal{L}$(1 MHz)=-112 dBc/Hz for the test oscillator used here. With some real experience of the matter I have come to the justified conclusion that a general-purpose commercial phase-noise measurement system is a necessity for frequency synthesis research.

In addition to the actual measurement method, the measurement environment also degrades the phase noise results. In particular, noise in the power supply rail, in the bias voltages and currents, and in the tuning node transfers into degraded phase noise. It is a good habit to use batteries as a supply source for phase noise measurements. Furthermore, one should try to generate the required bias currents with an external shielded tunable resistor bank instead of "universal source"-type laboratory equipment. I have observed improvements of over 20-dB as a result of the proper choice of sources. Obviously, this is related to the sensitivity of the circuit to external disturbances. Additionally, in some cases shielding improves the results significantly, although care is needed. Improperly designed shielding may actually cause the results to deteriorate.

2.4.4 Phase Noise – Tuning Range – Power Consumption Dilemma

Previous analysis of phase noise shows an interrelationship between power, frequency, and phase noise. On the basis of this a commonly used figure-of-merit (FOM) for oscillators is

$$FOM = 20\log\left(\frac{f_{osc}}{f_m}\right) - \mathcal{L}(f_m) - 10\log\left(\frac{P_{DC}}{1mW}\right) \tag{2.47}$$

This FOM definition is widely accepted and commonly used for benchmarking oscillators, but its results are occasionally misunderstood. The definition has some shortcomings. First, parameter relationships are not linear in real circuits. For instance, simply increasing the DC power does not necessarily improve phase noise. Furthermore, it is usually more difficult to achieve a good FOM value at higher frequencies. Second, the technology that is used is not considered. The technology has a strong impact, not only via the resonator Q-value, but also as a result of power consumption. Early silicon RF IC VCOs had a FOM ~ 160 dB, and the recent best circuits achieve a FOM ~ 190 dB. Third, the VCO tuning range is not taken into account and this is an often-neglected deficiency. The tuning range poses a problem for the FOM definition. In the most simplified analysis the tuning range has no impact on the phase noise. If we alter L or C in the LTI phase noise analysis, nothing happens. However, as soon as we face

the real world, the phase noise and tuning range are interrelated. The VCO phase noise and often also the power consumption get worse with a wide tuning range. However, this relationship is not clear. In simple single variable capacitor oscillators a wide tuning range implies a large tuning gain (K_{VCO}). Now, noise in the tuning node converts into increased phase noise. The higher the gain, the worse the phase noise. On the other hand, if a wide tuning range is achieved with multiple parallel tuning elements, such as a combination of a switched capacitor network and a single continuously tunable capacitor, we do not observe as clear a dependency between the tuning range and phase noise. In real oscillator design the challenge is thus to meet a high FOM with a wide tuning range. It is actually quite surprising to meet this relationship again and again in oscillator research. For instance, the tuning range – phase noise trade-off is observed in the following cases.

- Circuit structure: circuits with an inherently wide tuning range, such as ring oscillators or multivibrators, have a high phase noise level, while circuits with a low phase noise, such as crystal oscillators, have a narrow tuning range.
- In Nguyen's two-resonator oscillator [2.89] the tuning range is inversely related to the Q-value of the resonator, and thus the phase noise and tuning range are competing objectives.
- Device size: increasing the size of the oscillating device while maintaining the same power level usually improves the phase noise and, as a result of increased parasitic capacitance, reduces the tuning range.
- Monolithic inductor: using wider metal in an inductor reduces series resistance, thus increasing the Q-value but also the parasitic capacitance. In an oscillator we observe a tuning range – phase noise trade-off.
- Varactor: pn-junction varactor structures that have the highest Q-value also suffer from large parasitic capacitance. In MOS-varactors the Q-value and tuning range are both related to the device length (L) but in the opposite manner. Thus, the choice of the varactor length results in a phase noise – tuning range trade-off.
- In MOS switched capacitor networks the ratio C_{ON}/C_{OFF} impacts on the tuning range, but improving this ratio reduces the Q-value. Thus, we have a phase noise – tuning range trade-off.

We can summarize this discussion by noting that oscillator FOM is, in practice, related to the tuning range. Furthermore, die area plays a role too. A simple example is to consider an oscillator with a wide tuning range, and compare it to two parallel oscillators that have a narrower and slightly overlapping frequency ranges. The latter case shows a higher FOM, with a penalty of twice as large a die area. Another example is to consider noise reduction in NMOS oscillators with the LC-filtering technique [2.90]. The phase noise is reduced, but with a penalty of an increased die area. The ultimate goal of the RFIC VCO designer is to develop a VCO with a sufficient tuning range, the highest FOM, and a small die area.

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3 Reactive Feedback Oscillators

In this thesis LC oscillators are divided into two categories: circuits with a reactive feedback network for creating the negative resistance, and circuits where the active device is in a unity-feedback arrangement. Reactive feedback oscillators are studied first, purely for historical reasons. At the dawn of our art active devices were very expensive, while passive components were readily available and could even be manufactured by oneself in a workshop. This explains why reactive feedback oscillators were favored in the old days. Figure 3.1 depicts four classic oscillators, all invented during the decade after 1910, and named after their inventors [3.1]-[3.4]. Later, many alternatives were invented, and some of those are shown in Figure 3.2. In these figures I have included the simplest possible biasing into the circuits, so that all these circuits are real oscillators as they are now drawn.

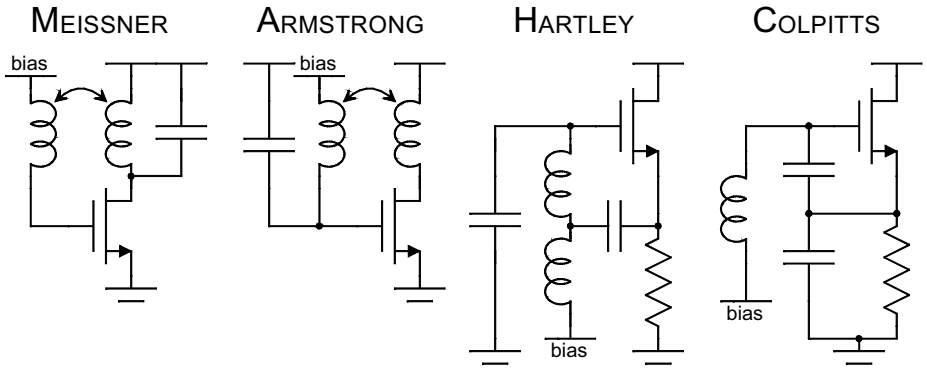


Figure 3.1. Four classic oscillators.

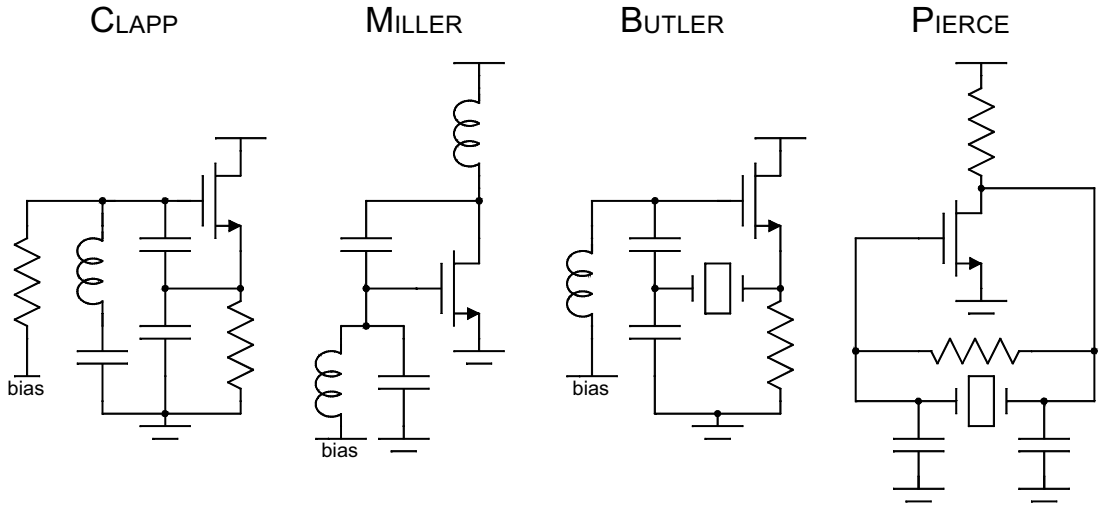


Figure 3.2. Some well-known oscillator topologies. The Clapp oscillator [3.5] is a popular extension of the Colpitts oscillator. Both parallel and series resonance are utilized. Gouriet [3.6] invented the same idea independently, and therefore this circuit is occasionally called a Gouriet-Clapp oscillator [3.7]. Even prior to these inventors Llewellyn used additional series reactance to improve frequency stability [3.8], [3.9]. The Miller oscillator is an extension of the Hartley oscillator, although it is usually represented as a crystal oscillator. The Pierce [3.10] and Butler [3.11] oscillators are also usually used as crystal oscillators. It is possible to replace the crystal with an LC series resonator in these schematics.

3.1 Structural Principles

Figure 3.3 depicts a generalized parallel network surrounding an active element and, as an example, a circuit analyzed by Jen [3.12]. In the generalized form of a reactive feedback oscillator each admittance Y can include a single reactive element or more complex circuitry. The active device Q can be any circuit providing gain, but here we consider it to be a single transconductance-type device, such as a vacuum tube, bipolar transistor, field-effect transistor, or a yet unknown future device. So as to avoid messy repetition of all the terminal type names, the nomenclature related to field-effect transistors (FET) will be used. The ground node can be at any of the three terminals, and correspondingly the device is in the common-drain, common-source, or common-gate configuration.

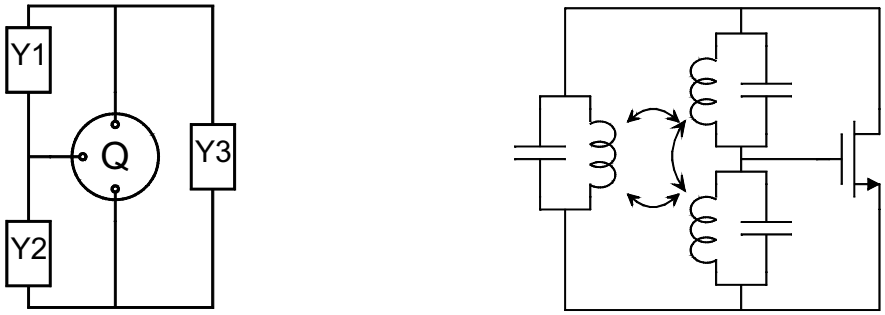


Figure 3.3. On the left, the general structure of a parallel reactive feedback oscillator. On the right, Jen's general circuit without bypass capacitors and biasing.

The active device is modeled as a transconductance g_m with the input (gate-source) admittance Yi, output (drain-source) admittance Yo, and feedback (gate-drain) admittance Ym. The characteristic determinant can be derived from the small-signal equivalent network, and by setting it to be equal to zero we find the characteristic equation for each circuit. Figure 3.4 depicts such an equivalent network for a parallel-type common-drain oscillator. Table 3.1 includes the characteristic equations for the three parallel feedback cases. The admittances Y2 and Y3 should be of the same type, while Y1 is of the opposite type. For instance, if Y2 and Y3 are capacitors, the circuit is the well-known Colpitts oscillator.

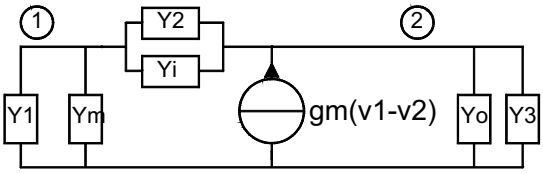


Figure 3.4. Small-signal equivalent network for parallel-type common-drain oscillator.

Table 3.1. Characteristic equations for the three parallel oscillators.

Oscillator configuration	Characteristic equation	Impact of parasitic
Parallel-type common-drain	(Y1+Y2)(Y2+Y3+gm) – Y2(Y2+gm) = 0	Y1 → Y1+Ym Y2 → Y2+Yi Y3 → Y3+Yo
Parallel-type common-gate	(Y1+Y3)(Y2+Y3+gm) – Y3(Y3+gm) = 0	Y1 → Y1+Ym Y2 → Y2+Yi Y3 → Y3+Yo
Parallel-type common-source	(Y1+Y2)(Y1+Y3) – Y1(Y1-gm) = 0	Y1 → Y1+Ym Y2 → Y2+Yi Y3 → Y3+Yo

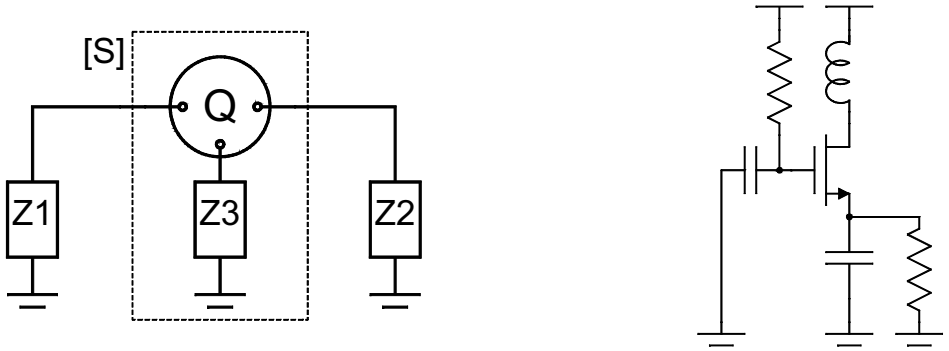
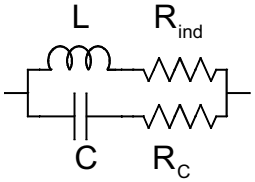


Figure 3.5. On the left, the series feedback oscillator concept, and the concept of two-port oscillator design. On the right, an example of a series feedback oscillator.

Figure 3.5 actually includes two principles. In the series feedback oscillators the three feedback impedances Z1, Z2, and Z3 surround the active device Q. This approach is a counterpart to the parallel feedback case. If we use this principle to create oscillators with the lowest device count, we end up with very similar circuits as in the parallel case. The six basic cases are analyzed in [3.13]. Note that in the series feedback case it is actually required that the active device has parasitics. For instance, the example circuit in Figure 3.5 does not oscillate if the active device is just a pure transconductor. If we consider the drain-source capacitance to be a part of the resonator, and the capacitance in the gate to be a bypass capacitor, then this circuit is the common-gate Colpitts oscillator. A design method commonly presented in microwave engineering literature is the two-port oscillator concept. In this method the active device is usually described with an S-parameter matrix. Often, additional internal feedback, such as an inductor at the gate terminal or a capacitor at source, is used to increase the potential instability of the active device. The output impedance (Z2) is chosen to be such that the impedance at the opposite port has a negative real part. Then a proper resonator (Z1) is chosen. In particular, when this methodology is applied to micro-strip designing, a large variety of circuit topologies emerges.

Yet another perspective on the variety of oscillator topologies is achieved by considering an amplifier in a feedback loop. If the phase shift over the loop is 180 degrees at a frequency where the amplifier still has gain, the circuit oscillates. The Pierce oscillator in Figure 3.2 is a simple example of such a circuit arrangement. In general, the resonator can be of any order as long as it provides proper phase shift. Furthermore, the amplifier can have more than one stage and, correspondingly, the phase shift that is required and hence the structure of the resonator will vary. From this way of thinking it is easy to understand that almost any amplifier structure and any resonator can be configured into an oscillator, leading to a large number of alternatives.

3.1.1 Resonators



$$\omega_{res} = \sqrt{\frac{1-\frac{C}{L}R_{ind}^2}{LC - C^2 R_C^2}} \tag{3.1}$$

Figure 3.6. Parallel LC resonator with losses and equation for the resonance frequency.

A basic parallel LC-resonator is depicted in Figure 3.6. At the resonance frequency, given by Equation 3.1, the imaginary part of the admittance is zero. Series resistance in the inductor lowers the resonance frequency and series resistance in the capacitor increases it. Any parallel loss element can be de-embedded from the resonator, and thus has no impact on the resonance frequency. The quality factors for the inductor and capacitor are

$$Q_L = \frac{\omega L}{R_{ind}} \qquad and \quad Q_C = \frac{1}{\omega C R_C} \tag{3.2}$$

With an approximation $\omega^2 = \frac{1}{LC}$ the resonance frequency is approximated with

$$\omega_{res} \approx \sqrt{\frac{1 - 1/Q_L^2}{LC\,(1 - 1/Q_C^2)}} \tag{3.3}$$

This result reveals that in most practical cases with reasonable Q-values we may neglect losses when considering the resonance frequency. Equation 3.1 must be used for very low-Q cases.

Basic reactive feedback oscillators, i.e. Colpitts and Hartley, are derived from the basic LC-resonator by dividing either the capacitor or the inductor into two segments. The reactive voltage divider then forms a feedback loop in the oscillator configurations. Figure 3.7 depicts various extensions of the basic configurations. Next we will briefly compare these structures and a simple common-drain oscillator is used as a test vehicle.

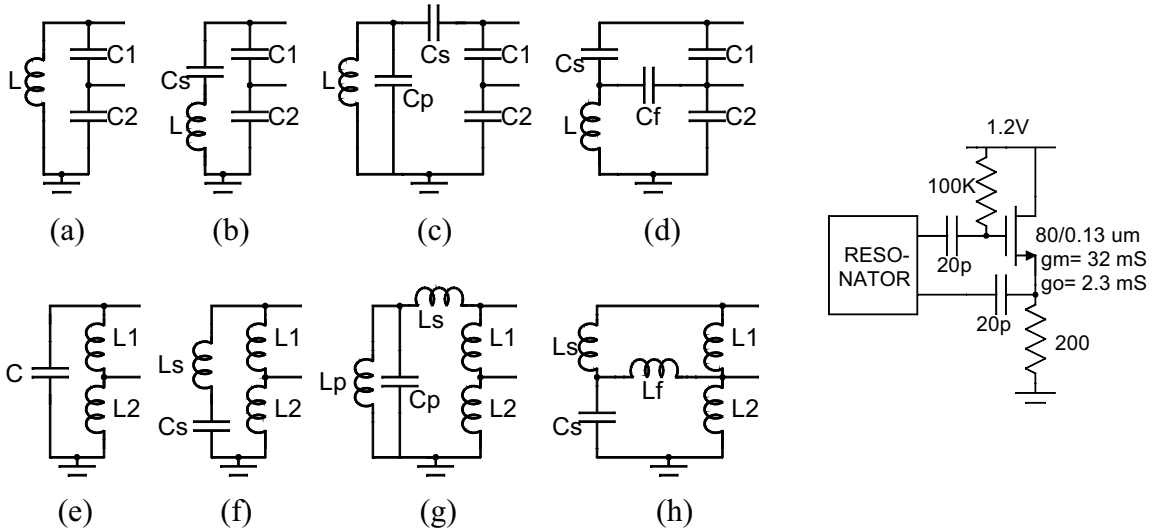


Figure 3.7. Some extensions of capacitive divider resonator are shown in the upper row. These are (a) Colpitts, (b) Clapp, (c) Seiler [3.14], and (d) Vackar [3.15],[3.16]. Resonators with an inductive divider are in the lower row: (e) Hartley, (f) Lampkin [3.17], (g) inductive counterparts of Seiler, and (h) inductive counterparts of Vackar. On the right, the schematic of the test oscillator is shown.

The resonance frequency of the Colpitts resonator is

$$\omega_{res} = \sqrt{\frac{1}{L\dfrac{C_1 C_2}{C_1 + C_2}}} \tag{3.4}$$

In oscillator analysis we can divide the circuit into the negative impedance port and the load port. Here, in the case of the Colpitts oscillator, the inductor L with a series resistance R_{ind} is the load and the negative impedance Z_g seen in the gate terminal and capacitive frequency divider is

$$Z_g = \frac{-g_m + \frac{C_1}{C_2}G}{\omega^2 C_1 C_2 + \frac{C_1}{C_2}G^2} - j\frac{1}{\omega}\left[\frac{\omega^2 C_1 C_2 + \frac{C_1}{C_2}G^2}{\omega^2(C_1+C_2) + \frac{G}{C_2}(G+g_m)}\right]^{-1} \tag{3.5}$$

G includes the bias resistor R_{bias} from the source to the ground and the output conductance of the FET ($G=1/R_{bias}+g_o$). The gate-to-source input capacitance is embedded into C_1. The terms in the above equation are often of the same magnitude, but to simplify the result we consider an ideal case G=0, and then we have

$$Z_g = \frac{-g_m}{\omega^2 C_1 C_2} - j\frac{1}{\omega}\left[\frac{C_1 C_2}{C_1 + C_2}\right]^{-1} \tag{3.6}$$

Furthermore, by substituting Eq. 3.4 (ω^2) into the above, we obtain

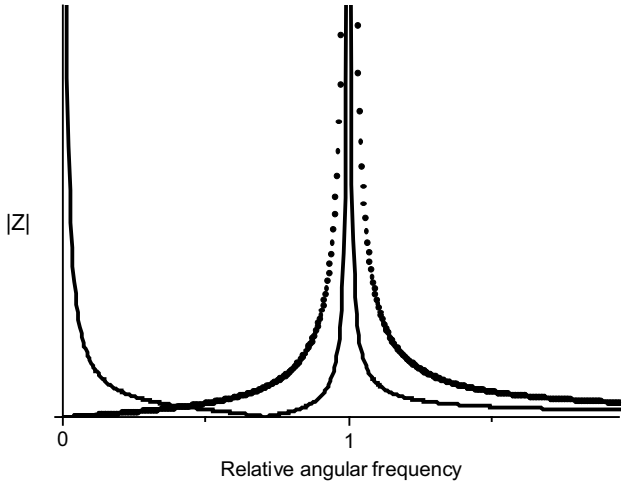
$$\mathrm{Re}\{Z_g\} = -g_m \frac{L}{C_1 + C_2} \tag{3.7}$$

Now the oscillation start-up condition is simply $\mathrm{Re}\{Z_g\} + R_{ind} < 0$. Often, the series resistance R_{ind} scales linearly with the inductance value L, and in such cases small capacitance values are beneficial. On the other hand, then the parasitics of the active device have a greater impact, which usually leads to worse frequency stability and the risk of an incorrect oscillation frequency.

In the Clapp resonator (Fig. 3.7b) an additional series capacitor C_s is included. The resonance frequency is

$$\omega_{res} = \sqrt{\frac{1}{L\frac{C_s C_1 C_2}{C_s(C_1+C_2)+C_1 C_2}}} = \sqrt{\frac{1}{LC_s\frac{1}{1+C_s\frac{C_1+C_2}{C_1 C_2}}}} \tag{3.8}$$

This result shows that if C_1 and C_2 are set to be much larger than C_s, the resonance frequency is defined by the series resonance L-C_s. However, Equation 3.7 indicates that lower negative resistance is achieved if the capacitors in the voltage divider are larger. For any meaningful use of the series resonator this factor should be at least four or five, and then correspondingly the g_m of the active device should be equally larger. Such a g_m is not necessarily available in RF IC cases and therefore the Clapp configuration is not well suited to low-Q inductors. As such, by adding more elements into the resonator the frequency response becomes steeper, thus improving frequency stability. A comparison of the Colpitts and Clapp resonators is depicted in Figure 3.8.



Clapp : continuous line

Colpitts : dotted line

Figure 3.8. Frequency responses of the Colpitts and Clapp resonators.

In the Seiler oscillator (Fig. 3.7c) a parallel resonator is used, and it is loosely coupled to the negative resistance circuit with a small series capacitor C_s. The resonance frequency of the resonator is

$$\omega_{res} = \sqrt{\frac{1}{L\,(C_p + \dfrac{C_s}{1 + C_s \dfrac{C_1 + C_2}{C_1 C_2}})}} \tag{3.9}$$

Just like in the Clapp oscillator, here too a higher resonator Q-value is needed compared to the basic Colpitts type. Good performance is usually found when $C_p<C_s<C_1<C_2$. This also means that large inductor values are needed.

The Vackar oscillator (Fig. 3.7d) is an extension of the Clapp oscillator. The additional feedback capacitor C_f couples the LC series resonator and the reactive voltage divider. The resonance frequency for the Vackar's arrangement is

$$\omega_{res} = \sqrt{\frac{1}{L\,(\dfrac{C_s C_1 C_2 + C_f C_1 C_2 + C_s C_f C_2}{C_s C_1 + C_f C_1 + C_s C_f + C_1 C_2 + C_s C_2})}} \tag{3.10}$$

In the Vackar circuit the capacitor C_f is tunable and according to Vackar's analysis [3.16] it is able to provide wider frequency tuning with almost constant characteristics compared to the other alternatives.

The Hartley oscillator (Fig. 3.7e) is the basis for circuits with an inductive voltage divider. From the small-signal equivalent circuit we can derive the determinant of the Y-matrix. Here it is best to represent inductor losses with parallel conductors G_1 and G_2.

$$\begin{vmatrix} j\omega C + Y_{in} + \dfrac{1}{j\omega L_1} + G_1 & -G_1 - Y_{in} - \dfrac{1}{j\omega L_1} \\ -G_1 - Y_{in} - \dfrac{1}{j\omega L_1} - g_m & \dfrac{1}{j\omega L_2} + G_2 + Y_o + \dfrac{1}{R_{bias}} + g_m + \dfrac{1}{j\omega L_1} + G_1 + Y_{in} \end{vmatrix} = 0 \tag{3.11}$$

To avoid cumbersome results we consider a case where the transistor is modeled only with a transconductance element and output conductance element, that is, $Y_{in}=0$. This leads to the following oscillation frequency and g_m required for sustained oscillation.

$$\omega_{osc} = \sqrt{\frac{1}{C(L_1 + L_2) + L_1 L_2 G_1 (G_2 + g_o + 1/R_{bias})}} \tag{3.12}$$

$$g_m > G_1 \frac{L_1}{L_2} + (G_2 + g_o + \frac{1}{R_{bias}}) \frac{L_2}{L_1} \tag{3.13}$$

By defining $\theta = L_1/L_2$, ($\Rightarrow G_2/G_1 \approx \theta$) and substituting these into Equation 3.13, we get

$$g_m > G_1 \theta + \frac{g_o + 1/R_{bias}}{\theta} + G_1 \tag{3.14}$$

The minimum requirement for g_m is met when

$$\theta = \sqrt{\frac{g_o + 1/R_{bias}}{G_1}} \tag{3.15}$$

Often, the ratio L_1/L_2 is in the range 1/3 … 1/2.

The extensions of the Hartley oscillator can be analyzed with the same methods as were used previously for the Colpitts derivatives, but these simple analysis results are omitted here to keep this section in a reasonable length.

Some practical insights into the differences of the resonators can be gained by simulating all the cases shown in Figure 3.7 with the same oscillating amplifier. The schematic, with the device sizes, is depicted on the right in Figure 3.7. In this simulation example the passive devices have characteristics that are common to modern IC technologies. The capacitors are high-Q devices with parasitic capacitance on both terminals ($C/C_{par}=10$). A 4-nH coil with 4-Ω series resistance and 0.1-pF parasitic capacitance in both terminals is used as an example of a typical monolithic coil. Linear parameter scaling according to the device sizes is then applied. Details of the characteristics of the monolithic coils and capacitors will be presented in chapters five and six.

This simple comparison demonstrates that quite a similar performance is achieved in all cases. No immediate improvement on the performance is achieved with more complex resonator types. Although an increment of the resonator order may in some cases improve the oscillator performance, in practice it also increases the risk of unwanted behavior. For instance, in the Hartley-type oscillators incorrectly modeled (ignored) mutual coupling of the inductors causes unexpected behavior. Generally, it has been, and still is, a good idea to keep to simple structures.

Table 3.2. Common-drain NMOS oscillators with resonators depicted in Figure 3.7. Active device is an 80/0.13-μm N-type MOSFET, supply voltage is 1.2 V, and the component values of the bias circuitry are given in Figure 3.7.

Circuit	Resonator dimensions	Freq [GHz]	I_{DC} [mA]	$V_{osc,gate}$ [V_{pp}]	$THD_{5,\ gate}$ [dBc]	N/C@1MHz [dBc/Hz]	FOM [dB]
Colpitts	L=4nH C1=2pF, C2=6pF	1.90	3.9	0.72	-27	-124	183
Clapp	L=8nH, Cs=1.5pF C1=2pF, C2=6pF,	1.88	3.2	0.18	-34	-121	181
Seiler	L=4nH C1=2pF, C2=4pF Cs=3.5pF, Cp=0.3pF	1.94	3.2	0.25	-34	-121	181
Vackar	L=6nH C1=2pF, C2=4pF Cs=2pF, Cf=0.1pF	1.89	3.2	0.27	-32	-121	180
Hartley	L1=2nH, L2=2nH C=1.4pF	1.94	3.4	0.76	-29	-122	182
Lampkin	L1=2nH, L2=2nH Ls=1nH, Cs=1.2pF	1.91	3.4	0.68	-31	-123	183
Ind-Seiler	L1=2nH, L2=2nH Ls=1nH, Lp=8nH Cp=1.7pF	1.94	3.2	0.41	-40	-122	182
Ind-Vackar	L1=2nH, L2=2nH Lf=8nH, Ls=1nH Cs=1.1pF	1.95	3.2	0.53	-37	-120	180

3.1.2 Differential Structures

Figure 3.9. Principle of differential oscillators. On the left, a connection perpendicular to the symmetry axis and on the right a pair of crossed connections.

A differential oscillator can be synthesized from a basic LC-oscillator by connecting one or several of the ground nodes together. At the symmetry line the nodes are then virtual ground nodes. Oscillators can be coupled together perpendicular to the symmetry axis or with pair of crossed connections, as shown in Figure 3.9. Basically, the properties of the differential oscillator circuits are the same as for the single-ended circuit, with the additional benefits of differential outputs and virtual ground nodes. These circuits can be analyzed by considering the operation in the differential and common modes. Usually, the target is to operate the oscillator in the differential mode, and ensure that the circuit remains stable in the common mode. Figure 3.10 depicts single-ended and corresponding differential common-gate Colpitts oscillators. Simulation results for these circuits are given in Table 3.3. We see that the results are equal. A 3-dB improvement in phase noise is exactly according to the theory since power consumption

is also doubled. Generally one may expect some improvement in the close-in phase noise since as a result of the symmetry properties the even-mode distortion and noise up-conversion are smaller. Figure 3.10 also shows the presence of the ground and supply rail impedances Z_{gnd} and Z_{vdd}. These impedances are due to on-chip interconnections, bonding wires, pads, package leads, and connections in a printed-circuit board. In general, these impedances are complex and difficult to predict exactly, and may vary according to the assembly process. Actually, it is a challenging task to define exactly where the zero-potential of the signal ("the ground") is. Figure 3.11 depicts how the oscillation frequency depends on the ground node inductance L_{gnd} (i.e. $Z_{gnd} \rightarrow L_{gnd}$). The single-ended case shows high dependency, while the differential case is immune to rail impedances. Even with an extreme value of C_{vdd}=100pF, there is still some variation, and actually it is therefore better not to minimize the ground impedance. A study of the effect of supply rail impedance reveals similar behavior. In real differential circuits there is always some device-to-device spread, and therefore the balance is not perfect. Even under a significant imbalance a differential circuit still remains far more immune to the rail impedances than a single-ended circuit. For instance, a 50-% deviation in the bias resistors R_{bias} of the circuit shown in Figure 3.10 still results in a circuit that has less than 1-MHz frequency deviation in a simulation similar to what is depicted in Figure 3.11. Even alone, this intricate problem of the rail impedances is a good reason to favor differential structures. There are other factors as well and the pros and cons of differential structures are summarized in the next list.

Pros and cons of differential oscillators

- Differential oscillators are almost immune to reactive rail impedances.
- Differential oscillators have lower sensitivity to noise in the supply and ground rails.
- Differential oscillators offer improvements with regard to phase noise.
- Differential oscillators provide accurate differential output signals.
- In differential oscillators the output waveform is less distorted.
- Differential oscillators need fewer by-pass capacitors (C_{vdd} and C_{bp} in Figure 3.10).
- In differential oscillators one capacitor may be halved (C_{22} in Figure 3.10).
- Differential oscillators consume twice as much current.
- Die area: differential oscillators have two resonators, but fewer by-pass capacitors.

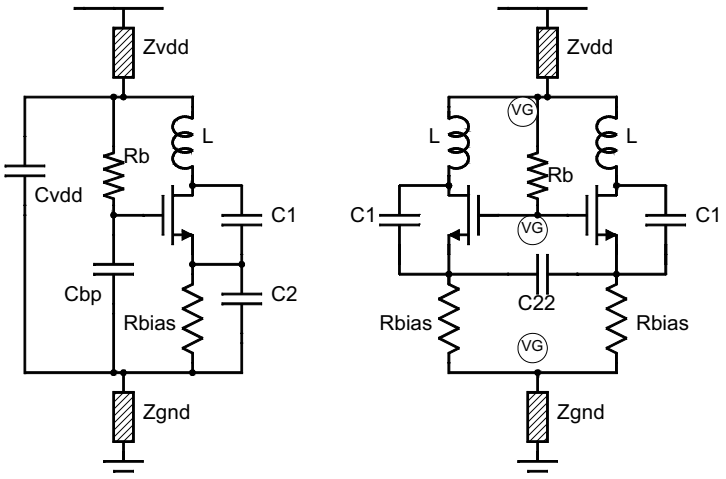


Figure 3.10. Single-ended and corresponding differential common-gate Colpitts oscillators. The symbol VG emphasizes the presence of a virtual ground node.

Table 3.3. Simulation results for the circuits shown in Figure 3.10.

Circuit	Freq [MHz]	I_{DC} [mA]	V_{osc} drain [V_{pp}]	THD_5 drain [dBc]	N/C@10kHz [dBc/Hz]	N/C@10MHz [dBc/Hz]
Single-ended	2037	1.98	1.19	-31	-66	-139
Differential	2037	3.97	1.19	-35	-69	-142
Component values	FET=40/0.13μm, Rbias=300Ω, Rb=100kΩ, L=4nH/4Ω, C1=2pF, C2=6pF, C22=3pF, Cvdd=20pF, Cbp=20pF					

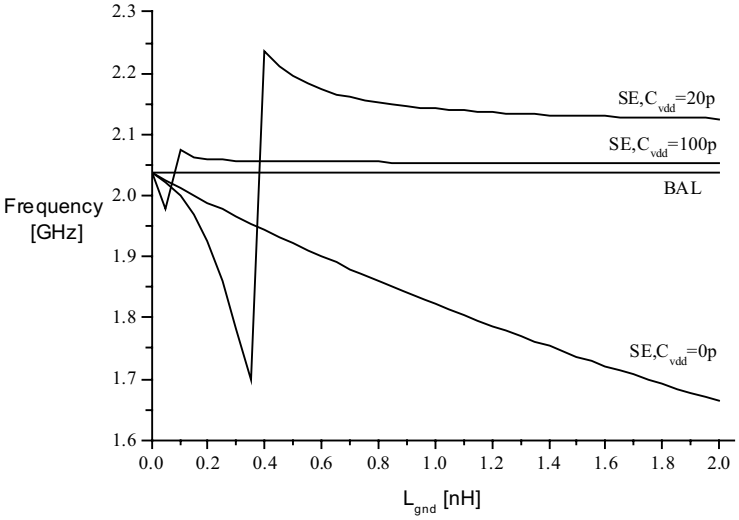


Figure 3.11. Impact of ground rail inductance on oscillation frequency. Differential (BAL) and single-ended oscillators with supply capacitor C_{vdd} values of 0 / 20 /100 pF are compared.

3.1.3 Best Oscillator Topology?

The aim of the discussion and analysis performed hitherto in this chapter has been to explain why we have such a plethora of oscillator circuit topologies and the aim has been to point out that the selection of "the best oscillator topology" is not a meaningful task. The best circuit topology depends on

- the implementation technology
- the performance requirements
- the design experience

The detailed arrangement of the LC resonator (e.g. Colpitts vs. Hartley) has only a mild influence on the overall oscillator performance. The results in Table 3.2 verify this. Furthermore, in a well-designed oscillator the active device acts almost as a switch [3.18],[3.19] and therefore the type of active device and its configuration also have just a moderate influence. There is no restriction on the complexity of the circuit structure and some performance increment might be available if the topology is enhanced. These three observations explain why we do not have a single winner among the oscillator topologies. On the other hand, a proper arrangement shows a significant performance increment over an arbitrary one, and thus it is a worthwhile task to seek the best candidate for a given technology and required performance. These improvements reveal mostly themselves in real large-signal situations, and it is not possible to derive generalized selection and design rules using linear analysis. Therefore, in the future too we will continue to see a plethora of oscillator structures and we will be forced to carry out their comparison in a case-by-case style.

3.2 Colpitts Oscillator

Within the history of oscillators the Colpitts oscillator is perhaps the most widely used oscillator topology. It is structurally simple, includes only one coil, and shows good performance in a wide range of applications. As discussed in the previous section, there is no formal proof of its superiority. It is practical issues, together with its good performance, that explain its dominance. Since it is the simplest reactive feedback oscillator structure that is also used in practice, its analysis is carried out here. The same analysis procedures used here can be applied to other oscillators as well. Many of the results are also more generally valid for other oscillators. We shall start by repeating the small-signal analysis of common-drain, source, and gate oscillators in more detail than in Table 3.1. Frequency tuning configurations are then compared. Next, analytical large-signal analysis methods are considered and phase noise analysis and simulations are shown. In the last section some design guidelines are provided.

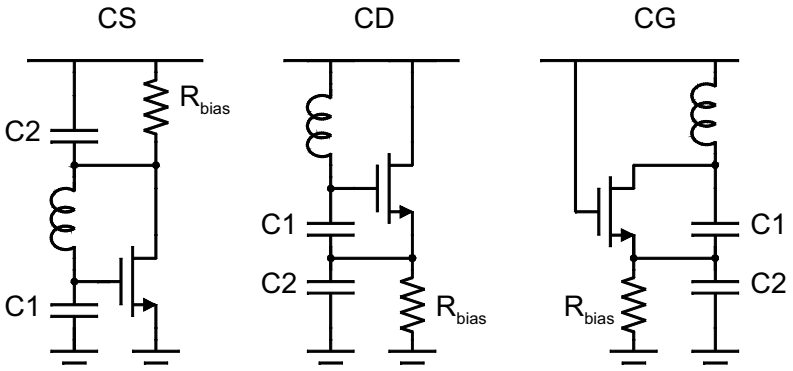


Figure 3.12. Colpitts oscillator in the common-source (CS), common-drain (CD), and common-gate (CG) configurations.

3.2.1 Linear Analysis

The small-signal analysis of these circuits starts by writing the characteristic determinant, as we did for the Hartley oscillator in Eq. 3.11. Inductor losses are represented with a parallel conductor G, capacitors are assumed to be lossless, and the gate-to-source capacitor is embedded into the actual capacitors C_1 or C_2. Inductor L with a series resistor R_{ind} has an equivalent parallel conductance

$$G = \frac{R_{ind}}{R_{ind}^2 + \omega^2 L^2} = \frac{1}{R_{ind}\left(1+Q^2\right)} \approx \frac{1}{R_{ind}Q^2} \tag{3.16}$$

A 4-nH inductor with 4-Ω series resistance has Q_{2GHz}= 13, and G= 1.6 mS.

From the real part of the characteristic equation we can solve the oscillation frequency, and the imaginary part gives us the requirement for the transconductance. It appears that the CD and CS cases are similar, while CG differs. For the CD and CS cases the oscillation frequency is

$$\omega = \sqrt{\frac{1}{L\dfrac{C_1C_2}{C_1+C_2}} + \frac{G\left(g_m + g_o + \dfrac{1}{R_{bias}}\right)}{C_1C_2}} \tag{3.17}$$

For the common-gate case we have

$$\omega = \sqrt{\frac{1}{L\dfrac{C_1 C_2}{C_1 + C_2}} + \frac{G\left(g_m + g_o + \dfrac{1}{R_{bias}}\right) + \dfrac{g_o}{R_{bias}}}{C_1 C_2}} \tag{3.18}$$

The transconductance requirements are

$$\text{for CD or CS} \qquad g_m > G\omega^2 L\left(C_1 + C_2\right) + \left(g_o + \frac{1}{R_{bias}}\right)\left(\omega^2 L C_1 - 1\right) \tag{3.19}$$

$$\text{and for CG} \qquad g_m > \omega^2 L C_1 (G + \frac{1}{R_{bias}}) + \omega^2 L C_2 \left(G + g_o\right) - g_o - \frac{1}{R_{bias}} \tag{3.20}$$

The first term in the oscillation frequency formula is usually 2-3 orders of magnitude larger than the second, and therefore we can safely manipulate the g_m-formulas by substituting only the first term. Furthermore, we define the capacitance ratio $\theta = C_1/C_2$. Now we have

$$\text{for CD or CS} \qquad g_m > G\left(2 + \theta + \frac{1}{\theta}\right) + \frac{1}{R_{bias}}\theta + g_o\theta \tag{3.21}$$

$$\text{and for CG} \qquad g_m > G\left(2 + \theta + \frac{1}{\theta}\right) + \frac{1}{R_{bias}}\theta + g_o\frac{1}{\theta} \tag{3.22}$$

Optimum values of θ for the minimum g_m requirement are

$$\text{for CD or CS} \quad \theta = \sqrt{\frac{G}{G + g_o + 1/R_{bias}}} \quad \text{and for CG} \quad \theta = \sqrt{\frac{G + 1/R_{bias}}{G + g_o}} \ . \tag{3.23}$$

All three cases have an equally simple design formula for the case $\theta = 1$

$$g_m > 4G + \frac{1}{R_{bias}} + g_o \tag{3.24}$$

Equations 3.21 and 3.22 reveal that the common-gate configuration is advantageous only if the output conductance is large, simultaneously with a large capacitance ratio. In other cases the three configurations are almost equal from the small-signal analysis perspective. Equation 3.23 indicates that the optimum design for high-Q and for low-Q resonators is different.

The comparison of different active device configurations can equally be performed with the negative conductance (resistance) method. All the three cases have the same input impedance

$$Z_{in} = \frac{g_m}{Y_1 Y_2} + \frac{1}{Y_1} + \frac{1}{Y_2} \tag{3.25}$$

If the admittances Y_1 and Y_2 correspond purely to the capacitors C_1 and C_2 then we have

$$Z_{in} = \frac{-g_m}{\omega^2 C_1 C_2} - j\frac{1}{\omega}\left[\frac{C_1 C_2}{C_1 + C_2}\right]^{-1} \tag{3.26}$$

If Y_1 and Y_2 include the active device parasitics C_{gs} and g_o, and the bias resistor R_{bias}, then the CD and CS cases are still equal, whereas the CG case differs. Moreover, if we study the impact of the gate resistor and the gate-to-drain capacitor further, then all three cases have different admittance related to these elements.

3.2.2 Frequency Tuning

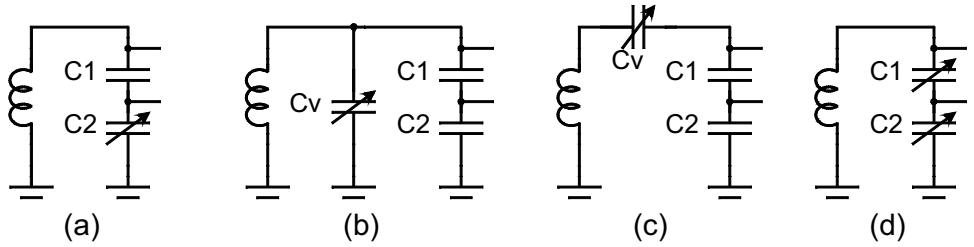


Figure 3.13. Four tuning methods for the Colpitts resonator.

Tuning a capacitor value is the most common way to vary the frequency of an LC-oscillator. The simple LC resonator shown in Figure 3.6 has the frequency tuning range

$$\frac{f_{\max}}{f_{\min}} = \sqrt{\frac{C_{\max}}{C_{\min}}} = \sqrt{\beta} \tag{3.27}$$

Figure 3.13 depicts four commonly used tuning configurations for the Colpitts oscillator. The tuning ranges are given next (tunable capacitor C_v ranges C … βC, and $\theta = C_1/C_2$).

for Case (a): $$\frac{f_{\max}}{f_{\min}} = \sqrt{\frac{\beta(\theta+1)}{\beta+\theta}} \tag{3.28}$$

for Case (b): $$\frac{f_{\max}}{f_{\min}} = \sqrt{\frac{\beta C_v + \frac{\theta}{\theta+1}C_2}{C_v + \frac{\theta}{\theta+1}C_2}} \xrightarrow{C_2 << C_v} \frac{f_{\max}}{f_{\min}} = \sqrt{\beta} \tag{3.29}$$

for Case (c): $$\frac{f_{\max}}{f_{\min}} = \sqrt{\beta\,\frac{C_v + \frac{\theta}{\theta+1}C_2}{\beta C_v + \frac{\theta}{\theta+1}C_2}} \xrightarrow{C_v << \frac{\theta}{\theta+1}C_2} \frac{f_{\max}}{f_{\min}} = \sqrt{\beta} \tag{3.30}$$

for Case (d): $$\frac{f_{\max}}{f_{\min}} = \sqrt{\beta} \tag{3.31}$$

Case (a) actually gives the smallest tuning range, but is commonly used in IC implementations because of its simplicity. Figure 3.14 illustrates a typical available tuning range as a function of

β and θ. Usually, θ<1 and β<3, and the VCO tuning range remains quite modest. Furthermore, Case (a) has a problem related to the tuning. Since the varactor is a part of the negative resistance generation circuit, the capacitance ratio θ varies with the tuning, and correspondingly the g_m requirement and thus the excess gain vary. The value of θ within the tuning range is

$$\theta = \frac{1}{\{1...\beta\}} \frac{C_1}{C_v} \tag{3.32}$$

This means that the oscillator characteristics vary with the tuning more than in other arrangements, and this effect is stronger for oscillators with a wide tuning range. Case (b) gives a wide tuning range if we have $C_2 << C_v$, which means in practice that C_v must be large and thus the operating frequency is low. This configuration is indeed in use in many discrete component designs. It can be used in RF ICs as well, but the tuning range tends to be narrow. In Case (c) the parasitic capacitance of the negative resistance is in series with the variable capacitance. Thus, the overall capacitance is smaller and the oscillation frequency is higher. Here the parasitic capacitance of the inductor and of the tunable capacitor itself limit the lowest practical value of Cv, and the resulting tuning range is often quite narrow. Case (d) is very attractive, but also has practical problems related to the device parasitics, DC biasing, and tuning. In a monolithic implementation varactors usually have large parasitic capacitance from one terminal to the substrate, see Chapter Six. The feasibility of Case (d) depends highly on the device characteristics.

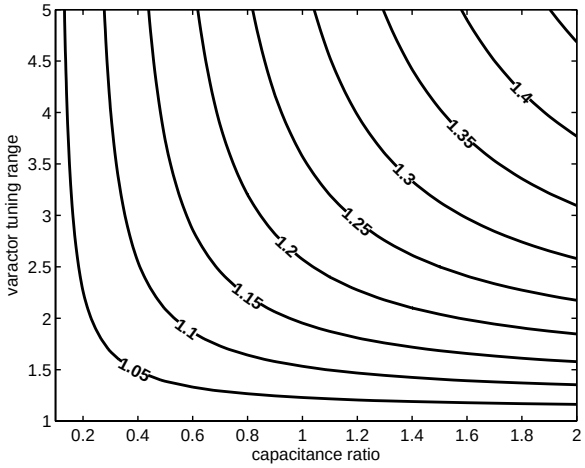


Figure 3.14. This contour plot depicts the tuning range of the Colpitts oscillator (Case a) as a function of the capacitance ratio θ and the varactor tuning range β.

3.2.3 Large-Signal Operation

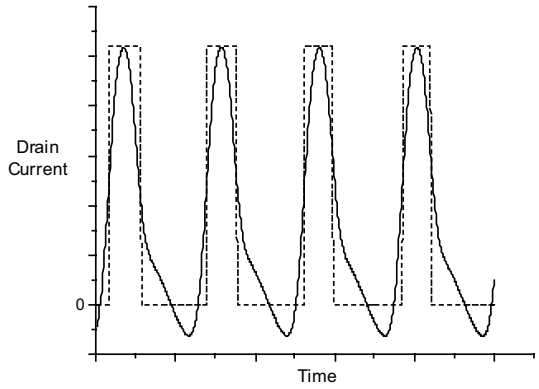


Figure 3.15. Drain current waveform in a CG Colpitts oscillator.

In principle, the large-signal behavior of an oscillator is determined with a set of differential equations. For the CG Colpitts oscillator the state equations are

$$\begin{aligned} C_1 \frac{dV_1}{dt} &= i_L - f(V_2) \\ C_2 \frac{dV_2}{dt} &= i_L - \frac{V_2}{R_{bias}} \\ L \frac{di_L}{dt} &= V_{DD} - i_L R_{ind} - V_1 - V_2 \end{aligned} \tag{3.33}$$

where *f(·)* represents the current of the active device. All the device parasitics are ignored. V_2 is the control voltage for the active device and therefore we rearrange the above DEs for V_2. The result is

$$LC_1C_2 \frac{d^3V_2}{dt} + C_1\left(\frac{L}{R_{bias}} + R_{ind}C_2\right)\frac{d^2V_2}{dt} + C_1\left(\frac{R_{ind}}{R_{bias}} + \frac{C_2}{C_1} + 1\right)\frac{dV_2}{dt} + \frac{V_2}{R_{bias}} - f(V_2) = 0 \tag{3.34}$$

Now we may test this formula by approximating *f(·)* with a simple third-order polynomial, as we did in the VDP case, and find an approximate solution by assuming that $V_2=A\cdot\cos(\omega t)$. This is mathematically straightforward and leads to a solution. Polynomial approximation of the behavior of the active device is used in some qualitative analysis for the transient behavior of the oscillator [3.20], [3.21]. However, in reality the Colpitts oscillator operates in class-C type mode, as depicted in Figure 3.15. The current waveform of the active device can be sinusoidal if high initial bias point is chosen and the excess gain is low. Such an oscillator shows poor performance, and therefore we ignore this uncommon case. This means that *f(·)* needs to take into account the operation of the active device in the on- and off-modes. For BJTs this is quite simple since the exponential current law is good for this purpose. However, the same exponential dependency means that the result (e.g. see at [3.22], [3.23]) includes modified Bessel functions and is therefore tricky to use. For FETs *f(·)* is even more complicated in the mathematical sense, and a solution to the DE problem is very hard to find.

A common approximate analysis method is to consider the waveform of the active device and derive the amplitude of the fundamental tone via Fourier transformation. Figure 3.15 depicts the drain-current waveform in a well-designed CG Colpitts oscillator. We may approximate the waveform with a constant current pulse with the duration $(\phi/2\pi)\cdot T_{osc}$. Among others, Mayaram [3.24],[3.25], Huang [3.26], and Abidi's group [3.27] have derived detailed results using this method. However, in the results of these authors the conduction angle ϕ remains in the final form of V_{osc}. So they are not actual closed-form results binding V_{osc} directly to the device sizes. In a simplified case we consider a basic common gate Colpitts oscillator biased with an ideal current source I_{bias}. The active device has a current waveform $i_{act}(t)$, and from the Fourier series presentation we can find the current amplitude of the fundamental tone. If $i_{act}(t)$ is a narrow pulse or actually a chain of pulses, these pulses appear at the maximum point of oscillation, and so we may approximate the cosine term in Equation 3.35 by unity. Furthermore, over the complete oscillation period the overall signal current must equal I_{bias}. So, we have

$$I_1 = \frac{2}{T}\int_0^T i_{act}(t)\cos(\omega_{osc}t) \approx \frac{2}{T}\int_0^T i_{act}(t) = 2I_{bias} \tag{3.35}$$

Now the situation is such that the active device feeds a current pulse into the resonator, and we know the level of the fundamental tone of this current. Higher harmonics are attenuated in a high-Q resonator, and therefore they are ignored here. In a common-gate Colpitts oscillator this

current is fed into the resonator through the common node of the capacitors C_1 and C_2. The oscillation amplitude appears over the effective parallel resistance of the resonator seen from this input node. Here that equals to $1/G_{reso}$ scaled with a parameter related to the capacitance ratio. Therefore, the final expression for the oscillation amplitude consists of the scaling factor, the fundamental current, and the parallel conductance, and is given by (see also [3.28])

$$V_{osc} = \left(\frac{1}{1+\theta} \right) \cdot 2I_{bias} \cdot \frac{1}{G_{reso}} \tag{3.36}$$

This result can be represented as

$$\boxed{V_{osc} = M \cdot I_{bias} \cdot Q_{reso} \cdot Z_0} \tag{3.37}$$

This is the generalized oscillator design formula. Here M is a factor carrying information on circuit topology, design choices (such as θ), and active device characteristics. Z_0 is the characteristic impedance of the resonator $\sqrt{L/C}$. Although here the formula was derived in an approximate manner, it appears to hold well with simulations, and agree with more detailed analysis. This formula is not accurate enough for actual circuit design. Instead, it is qualitative in nature, and should be used for considering design choices. Generally, oscillators may operate in two modes. In the current-limited region the equation holds, whereas in the voltage-saturation region oscillation swing is limited by some hard limits and cannot grow further. It is generally not a good idea to design an oscillator to operate in the voltage-saturated region. Some DC power is wasted, and excess current and stronger nonlinear operation increase the phase noise. So, this basic equation should be used with care to estimate the impact of design choices. For instance, we may double the resonator Q, and halve I_{bias} to maintain the same oscillation amplitude. Or we may increase Z_0 by increasing the size of the inductor, and equally reduce I_{bias}. Some simulation results are depicted in Figure 3.16 to clarify this discussion.

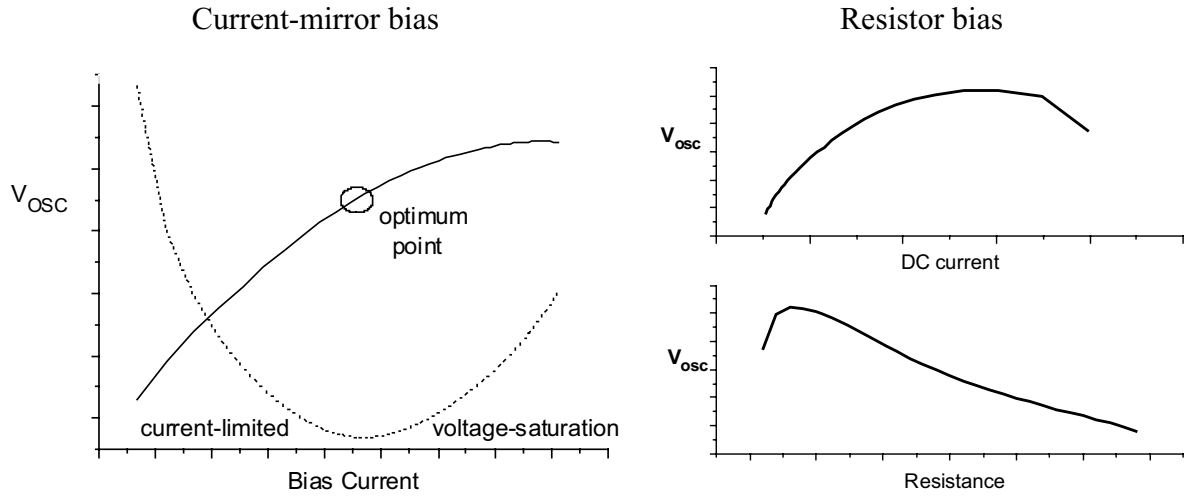


Figure 3.16. Performance of a CG Colpitts oscillator. On the left, bias current sweep for a current-mirror biased oscillator is shown, and on the right the oscillator is biased with a resistor. In the left-hand figure the circle symbol indicates an optimum design point. The dashed line depicts the phase noise.

3.2.4 Phase Noise

Prior to actual discussion of Colpitts oscillator phase noise, a brief reminder about the noise sources in the active devices is worth. Although these models will not be used to represent

detailed small-signal analysis here, it is important to acknowledge their role. The material here is based on Lee [3.28] and van der Ziel [3.29]. Various field-effect transistor types resemble each other in this aspect and only the MOSFET is studied here. The same applies for conventional BJT and heterostructure devices. The small-signal models of a FET and a BJT, including the dominant noise sources, are depicted in Figure 3.17.

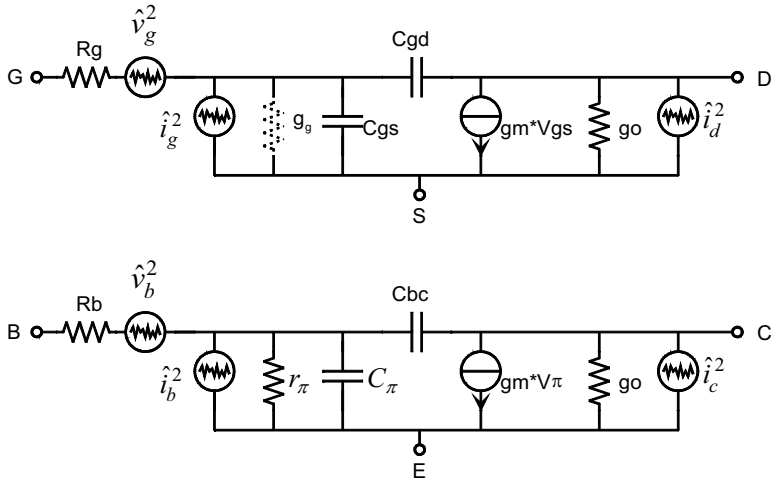


Figure 3.17. Small-signal models of a FET (upper) and a BJT (lower) including noise sources.

In a BJT the main noise sources are related to the base current I_b, collector current I_c, and base resistance R_b. The mean-square values for these sources are

$$\begin{aligned} \hat{i}_b^2 &= 2qI_b\Delta f + K\frac{I_b}{A_j}\frac{1}{f}\Delta f \\ \hat{i}_c^2 &= 2qI_c\Delta f \\ \hat{v}_b^2 &= 4kTR_b\Delta f \end{aligned} \tag{3.38}$$

where q is the electron charge, k is Boltzmann's constant, T is the absolute temperature, K is an experimental fitting parameter, and A_j is the base-emitter junction area. In BJTs 1/f noise (flicker noise) is, in practice, solely the result of the forward-bias base-emitter junction. The base resistor generates only thermal noise. This noise source can also be made to include the external noise impacting on the base terminal. As long as the base-collector leakage current is very small, the noise sources in a BJT are independent, and it is sufficiently accurate and a common habit to represent BJT noise sources as in Equation set 3.38. Correspondingly, the noise sources in a FET are

$$\begin{aligned} \hat{i}_g^2 &= 4kT\,g_g\,\delta\,\Delta f \qquad where \qquad g_g = \frac{\omega^2 C_{gs}^2}{5g_o} \\ \hat{i}_d^2 &= 4kT\,g_o\,\gamma\,\Delta f + K\left(\frac{g_m}{C_{ox}}\right)^2\frac{1}{W\cdot L}\frac{1}{f}\Delta f \\ \hat{v}_g^2 &= 4kTR_g\Delta f \end{aligned} \tag{3.39}$$

The gate noise coefficient δ has a value of 4/3 in long-channel devices, but for short-channel transistors it increases. Correspondingly, the drain noise coefficient γ is 2/3 and it increases as a result of high-field effects (velocity saturation and channel length modulation) in short-channel devices. These coefficients are bias-dependent and complicated indeed to model [3.30],[3.31].

The exact increment is not obvious and it seems to vary in different experiments. A factor of 4 is a good estimation for a 0.13-μm CMOS technology. Note that the noise conductance g_g is an instrument for noise analysis only. In contrast to r_π, it is not to be included into the small-signal analysis. In a FET the thermal agitation of the channel charge causes both the drain current noise and the induced gate current noise, and thus they correlate. Here g_o refers to the zero-bias output conductance. In saturation it is often replaced by a g_m with a factor of one for long-channel devices, but for small devices g_m/g_o is smaller than one [3.32]. These noise models are actually valid for the saturation (active) region only. In the off-state the transistor resembles a high-value resistor and generates only thermal noise. In this context we may say that transistors have negligible noise in their off-state. Since the gate (base) terminal noise is multiplied by the transistor gain, it is actually quite significant in RF circuits [3.31]. A large device with multiple fingers minimizes the gate (base) resistance. A large device also reduces the 1/f noise, as shown in the previous equations.

Considering the proper size of the active device, we may study the impact of device size by keeping the transconductance constant (in a FET transconductance $g_m \propto \sqrt{I_d \cdot W/L}$). It appears that the oscillation amplitude does indeed remain almost constant and the improvement of phase noise saturates with very large device sizes. So, a large device with a low bias point results in low phase noise with a low bias current, and is indeed beneficial but only down to a certain level.

The aim of the next analysis is to compare the small-signal based noise analysis to that of large signal analysis, and to point out that the validity of the linear analysis method is doubtful, and the results are therefore less accurate or even wrong. The main reason for this is that the small-signal analysis is not able to accurately describe all nonlinear behavior, such as the role of the cyclostationary noise sources. Yet, this type of analysis has been applied in various manners, e.g. [3.33]-[3.36]. All the noise sources in an oscillator can be converted into one equivalent noise source, and then, by applying the linear phase noise analysis discussed in Section 2.4.2, we can carry out an oscillator phase noise analysis. The total noise voltage for a series LRC presentation (Eq. 3.26) of the Colpitts oscillator depicted in Figure 3.18 is expressed as

$$\hat{v}_{tot}^2 = \hat{v}_{ind}^2 + H_1(\omega)\cdot\hat{v}_{gate}^2 + H_2(\omega)\cdot\hat{i}_{gate}^2 + H_3(\omega)\cdot\hat{i}_{drain}^2 + H_4(\omega)\cdot\hat{v}_{bias}^2 \tag{3.40}$$

Here $H_n(\omega)$ are the noise transfer functions. Unfortunately, even for the simplified CG Colpitts oscillator these functions are quite involved, and thus not instructive. Therefore, we rely on simulations here as well. The previous circuit analysis and simulations in this chapter have indicated that no major difference exists among the CS/CD/CG configurations. The noise sources in FETs and in BJTs have slightly different physical origins and typical levels, yet from the behavioral point of view they are close. Hence we may use an NMOS common-gate Colpitts oscillator as a test vehicle here without any significant loss of generality. Figure 3.18 depicts such an oscillator with the major noise sources visible. Table 3.4 depicts noise contributions in weak oscillation, at the optimum (lowest phase noise) point, and in the voltage-saturated mode. The small signal results are achieved with a linear noise analysis that gives the overall noise and noise contribution of each source, and with a time-domain simulation that gives us the oscillation amplitude. On the basis of the linear noise analysis presented in Chapter Two, phase noise is given by

$$\frac{N}{C} = \frac{\hat{v}_{tot}^2}{P_{osc}}\left(\frac{\omega_0}{2Q\omega_m}\right)^2 = \hat{v}_{tot}^2\left(\frac{\omega_0}{\omega_m}\right)^2\frac{R_{ind}}{4V_{osc}^2} \tag{3.41}$$

In the weak oscillation case both analysis methods show similar noise contributions, but when the oscillator is in the normal mode and the active device is on for only a part of the cycle, small-signal analysis fails to show proper contributions. This type of noise contribution analysis reveals that in the voltage-saturated region the oscillation amplitude does not grow any more, but the bias current and thus the noise, does grow, and therefore the phase noise increases. Furthermore, in the voltage-saturated region the oscillator behaves in a more nonlinear manner, which also explains the increased noise.

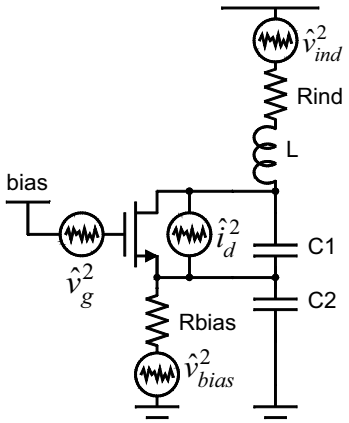
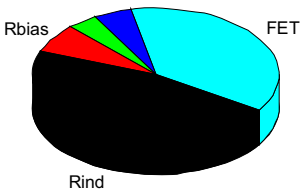
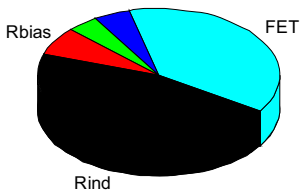
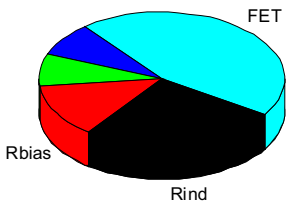
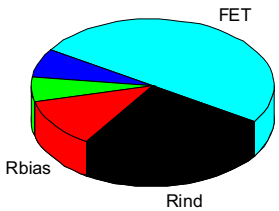
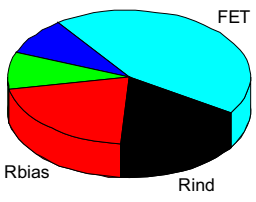
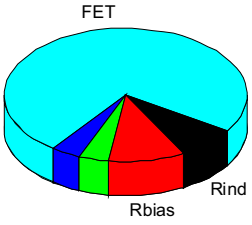


Figure 3.18. CG Colpitts oscillator with noise sources visible. In the example cases for noise simulations the device sizes are L=2nH/2Ω, C1=2pF, C2=4pF, FET=40/0.13 μm, the gate bias is 0.7V, and the supply is 1.2 V.

Table 3.4. Phase noise contributions in a 3-GHz CG Colpitts oscillator. Here the label FET includes both drain- and gate-induced noises. The two small slices are due to the gate resistance and source and bulk resistances.

Case	Small-signal simulation	Large-signal simulation
Weak oscillation V_{osc}= 0.14 V_{pp} ϕ= 100 %	 N/C @1MHz = -115 dBc/Hz	 N/C @1MHz = -102 dBc/Hz
Optimum V_{osc}= 1.5 V_{pp} ϕ= 40 %	 N/C @1MHz = -118 dBc/Hz	 N/C @1MHz = -120 dBc/Hz
Voltage saturated V_{osc}= 1.8 V_{pp} ϕ= 60 %	 N/C @1MHz = -118 dBc/Hz	 N/C @1MHz = -116 dBc/Hz

So far we have learnt that a large active device with a low bias point is the correct choice for high performance, and Equation 3.37 binds the inductance value and resonator quality factor to the proper bias current. The remaining task is to find out the optimum capacitance ratio θ. Considering the four different tuning arrangements depicted in Figure 3.13, if we let $\theta \rightarrow 0$, then Cases (a) and (c) actually collapse to TR=1. Anyway, for reasons of brevity we focus here on the basic Colpitts oscillator shown in Figure 3.18. The capacitance ratio θ impacts on all the major properties and is therefore intricate to study. First, the series connection of C_1 and C_2 acts as a voltage transformer and scales V_{osc}. Second, the transconductance requirement (Eq. 3.22) and thus the bias current requirement are influenced by θ. Third, the tuning range is a function of θ (Eq. 3.28). Fourth, the characteristic impedance Z_0 varies with θ. Finally, oscillation frequency is also a function of θ. Now, if we reduce the value of θ, the oscillation amplitude increases and the phase noise improves until the oscillator enters the voltage-saturated region. Then the phase noise performance begins to degrade. Bias current reduction can be used to compensate for the overly increased voltage swing, and then the optimum θ is found at a lower value. Eventually the bias current becomes so low and the g_m requirement so high that the oscillator fails to operate properly. Thus, we have an optimum value of θ for a given bias current, and also an overall optimum θ-I_{bias} setting does exist. This argumentation can be verified with simulations. Figure 3.19 depicts such a study. Margarit [3.37] uses the ISF theory to numerically derive a result similar to that in Figure 3.19. Theoretical analyses by Huang [3.38] and by Abidi's group [3.27] show the same type of dependency on θ. However, the theoretical works are not able to accurately describe the transition to the voltage-saturated region, and therefore these theoretical works are not able to provide an explicit design formula for the optimum θ. The optimum θ is usually found in the range ¼ to ¾, but there are cases, like the one in [3.39], where the optimum value seems to be above one.

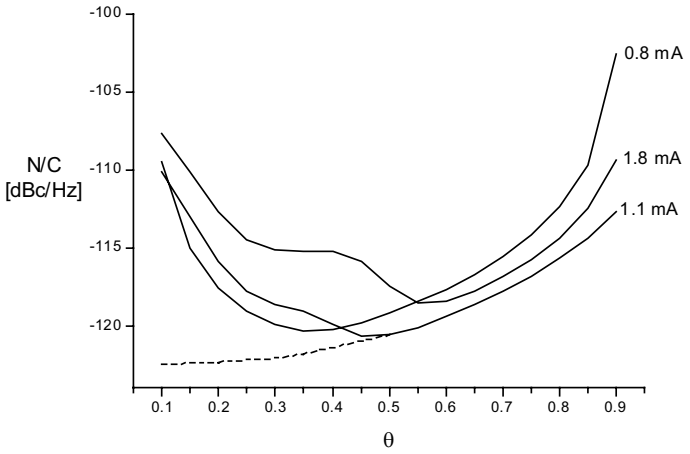


Figure 3.19. Phase noise as a function of capacitance ratio with three bias settings. The dashed line depicts how the phase noise would improve if the oscillator did not enter the voltage-saturation region.

On one hand the phase noise of the oscillator is strongly contributed by the noise of the active device, and on the other hand, the transistor operates in a switch-like manner in a well-designed oscillator. To gather some practical perspectives on this matter, Table 3.5 includes simulations of the same oscillator, depicted in Figure 3.18, with different active devices. In the PMOS cases the complete circuit is reversed. The bias point of the transistor and the size of the bias resistor are used as design parameters for achieving the lowest phase noise point. These results show that the type of the transistor does indeed have a minor effect. This explains and motivates the high level of activity in the development of resonator components.

Table 3.5. Properties of the oscillator in Figure 3.18 with different transistors.

Technology	transistor	Freq [MHz]	V_{osc} [V_{pp}]	I_{DC} [mA]	$\mathcal{L}$(10 kHz) [dBc/Hz]	$\mathcal{L}$(1 MHz) [dBc/Hz]	FOM [dB]
0.5-µm CMOS	NMOS	2770	1.8	2.3	-82	-122	186
	PMOS	2190	1.0	3.4	-78	-118	179
0.35-µm CMOS	NMOS	2970	1.7	2.1	-76	-121	186
	PMOS	2740	1.4	2.2	-77	-120	185
0.13-µm CMOS	NMOS	3040	1.6	1.6	-67	-120	187
	PMOS	2970	1.7	1.9	-71	-121	187
65-nm CMOS	NMOS	3070	1.8	1.9	-70	-119	185
	PMOS	3050	1.7	2.0	-74	-120	186
65-nm CMOS	NMOS	3060	1.6	1.4	-70	-119	186
	PMOS	3030	1.6	1.6	-71	-120	187
0.8-µm BiCMOS	NPN	2800	1.5	2.0	-77	-117	182
0.9-µm SiGe	NPN	2820	1.5	1.2	-77	-119	186
0.7-µm GaAs	D-MESFET *	2970	1.9	7.6	-80	-117	175
	E-MESFET	2970	1.6	2.2	-80	-120	185
0.5-µm GaAs	D-MESFET **	2920	1.6	5.1	-81	-121	181

* Vdd = 2V ** Vdd = 1.5V

3.2.5 Design Guidelines

General design guidelines for the design of a good Colpitts oscillator are difficult to give, since the performance requirements and implementation technology have a strong impact on the proper design choices. In particular, the tuning range that is required and the quality of the resonating elements lead the design choices. However, some general hints, valid for most cases, are provided below

- The CG/CD/CS configurations are almost equal, so choose according to ease of implementation. Usually, bias arrangements are different.
- Select the proper tuning method (Fig. 3.13); this depends on the tuning range requirement and on the device characteristics.
- Favor a differential structure even if single-ended output is desired.
- Maximize the resonator Q-value and use as large a characteristic impedance Z_0 as feasible. This does not mean that the largest coil would lead to the best performance.
- Use a large active oscillating device with a low bias point.
- Bias circuitry: minimize resonator loading, minimize additional noise.
- Check that sensitivity to supply rail fluctuations is low.
- Avoid operating an oscillator in the voltage-saturated region. The traditional rule "maximize V_{osc}" is actually not valid.
- Select a low capacitance ratio C_1/C_2. An optimum value for a given technology and targeted performance does exist.
- The output buffer should not load the resonator severely, and yet sufficient output power needs to be delivered.

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4 Unity Feedback Oscillators

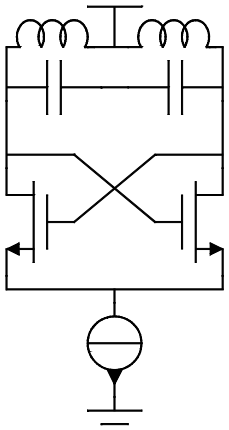


Figure 4.1. LC oscillator with tail-biased NMOS pair in unity-feedback arrangement.

When any transconductance type device is fed with an input signal that is an inverse of the output signal, the device shows negative resistance characteristics.

$$\begin{cases} i_{out} = g_m v_{in} \\ v_{in} = -v_{out} \end{cases} \quad \Rightarrow \quad R = \frac{v_{out}}{i_{out}} = -\frac{1}{g_m} \tag{4.1}$$

Obviously, in practice any real physical circuit needs proper biasing for feeding the energy provided by the negative resistance. By far the most common way to establish the unity feedback situation is to use a cross-coupled transistor pair (CCP). Here at the beginning, we will use a tail-biased NMOS pair as a basic circuit for analysis. Such circuit is depicted in Figure 4.1. Various biasing methods for this cross-coupled NMOS pair are studied in Section 4.2. Then, PMOS and CMOS CCP-circuits are introduced and a brief comparison of various structures is carried out. MOSFET devices are used here, just like in the previous chapter since fundamentally the type of active device has only a minor effect. However, now we need to look a little more closely at some specific details and therefore Section 4.4 is devoted to BJTs. Finally, this chapter ends up with a brief discussion of reactive feedback vs. unity feedback.

Historically, the concept of unity feedback is not as easily traced as was the case for the reactive feedback circuits. As such, the idea of differential circuits and cross-coupled connections appears in the early papers and patents, at least already in Meissner's patent [4.1]. The plate-coupled multivibrator, invented by Abraham and Bloch in 1919, has a cross-coupled connection but the circuit was not an LC oscillator. Later, an obvious enhancement of including a parallel LC resonator in it was made [4.2]. Herold presented a general discussion of negative resistance circuits in 1935 [4.3], and he classifies them into three groups, one being the "reverse phase coupled group", that is, the circuits studied here and in the previous chapter. For this group of circuits Herold simply states: "Most of this group is too well known to require even a brief discussion." Turner's "kallirotron" in 1920 (see [4.4],[4.5]) was one of the first circuits where cross-coupled devices were used for generating the negative resistance. An oscillator by Reich [4.5] in 1937 closely resembles the present-day CCP-circuits, and in his analysis Reich uses the same concepts and nomenclature that are common nowadays.

4.1 NMOSFET Cross-Coupled Pair

A basic cross-coupled NMOS transistor pair is depicted in Figure 4.1. As a result of its balanced nature the signals at the gates are equal but opposite in polarity, and the common-source node is a virtual ground node. Small-signal analysis using an equivalent circuit of a FET, including the terminal resistors gives us the single-ended input admittance seen from one drain terminal:

$$Y_{in} = \left[-\frac{g_m - j\omega C_{gs} R_s g_o}{1 + j\omega C_{gs}(R_g + R_s)} + g_o \right] \cdot \left[1 + R_d g_o + R_s g_o + R_s \frac{g_m - j\omega C_{gs} R_s g_o}{1 + j\omega C_{gs}(R_g + R_s)} \right]^{-1} \quad (4.2)$$

The role of the drain resistance is minor ($R_d g_o << 1$), and if we pay attention in the layout design to minimizing the source resistor R_s, we may approximate $R_d=0$ and $R_s=0$, and then the input admittance is

$$Y_{in} = -g_m \frac{1}{1 + j\omega C_{gs} R_g} + g_o \quad (4.3)$$

The role of the gate resistance R_g is particularly important. The only pole in the frequency response is caused by the $R_g C_{gs}$ product and if R_g is omitted the circuit has infinite bandwidth. If the terminal resistors are assumed to be small, we can see from the schematic that all the parasitic capacitors (C_{gs}, C_{gd}, C_{ds}, C_{db}, C_{gb}) can be embedded into the resonating capacitor. This explains why this particular circuit is able to provide very high oscillation frequencies, and it has indeed been used for benchmarking CMOS technologies. A 200-GHz oscillator is demonstrated with a 45-nm CMOS technology [4.6]. If the resonator losses are represented again by a parallel conductor G, then, ignoring the RC pole, the oscillation start-up conditions are simply

$$g_m > G + g_o \qquad \omega_{osc} = \sqrt{\frac{1}{L\left(C_{reso} + C_{par}\right)}} \quad (4.4)$$

For a crude estimation of large-signal behavior the argumentation follows the same track as with the Colpitts oscillator. We assume a certain shape for the drain current, such as a square wave or half-sinusoid, and this current flows through the resonator, resulting in the oscillation amplitude being proportional to the bias current and effective parallel resistance R_p of the resonator. A common habit when discussing this issue is to assume the drain currents to be of square wave type and then the single-ended oscillation amplitude is given by

$$V_{osc} = \frac{2}{\pi} I_{bias} R_p \quad (4.5)$$

So, these CCP-type devices also follow the generalized basic Equation 3.37. Furthermore, here too we can divide the operation into the current-limited and voltage-limited regions (see Figure 3.16). Unfortunately, generally speaking, the CCP circuits do not behave exactly as the idealized models assume. Thus, here too the role of Equation 3.37 remains qualitative. Figure 4.2 depicts drain current waveforms for a circuit depicted in Figure 4.1. As we can see, the waveforms are not close to the ideal case, and even worse, both transistors conduct at the same time. This means that while one transistor is considered primary and is in the active mode, the opposite transistor appears as an additional loss element drawing energy from the resonator.

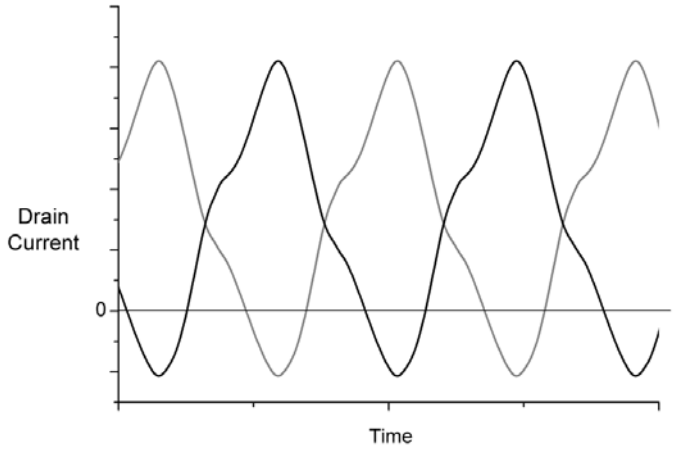


Figure 4.2. Drain current waveforms in an NMOS CCP oscillator.

The simple cross-coupled pair shows a differential negative conductance over an LC resonator, and is therefore a close representation of the VDP oscillator. Next, we will derive formulas to couple the VDP oscillator and CCP oscillator. In order to maintain reasonable simplicity, we restrict the analysis to the simple case where the FETs obey the square-law dependency

$$I_d = \frac{1}{2}K\left(V_{GS} - V_{TH}\right)^2, \qquad K = \mu_n C_{ox}\frac{W}{L} \tag{4.6}$$

By solving V_{GS} from the above equation, the differential input voltage for a FET pair is

$$v_{in} = V_{GS1} - V_{GS2} = \sqrt{\frac{2I_{d1}}{K}} - \sqrt{\frac{2I_{d2}}{K}} \tag{4.7}$$

The above equation is used for solving the differential current. A little manipulation leads to

$$i_{diff} = I_{d1} - I_{d2} = \tfrac{1}{2}Kv_{in}\sqrt{\frac{4I_{bias}}{K} - v_{in}^2} \approx \sqrt{K\,I_{bias}}\,v_{in} - \frac{1}{8}\sqrt{\frac{K^3}{I_{bias}}}\,v_{in}^3 + \ldots \tag{4.8}$$

The IV characteristic of a cross-coupled pair is obtained by inverting the polarity of the input voltage. From the Taylor series of Eq. 4.8 we are now able to identify the corresponding factors of the VDP polynomial $i(v) = -g_1 v + g_3 v^3$, and then Equation 2.11 gives the oscillation amplitude. We get

$$V_{osc} = \sqrt{\frac{32}{3K}}\sqrt{I_{bias} - (V_{GS} - V_{TH})\,G} \tag{4.9}$$

Three conclusions can be drawn. First, a minimum current for the onset of oscillation does exist. This corresponds to the small-signal result g_m>G. Second, a low bias point is beneficial. Third, the oscillation swing is proportional to $\sqrt{I_{bias}}$. This analysis has some shortcomings, though. First, we used a simple square law for the FETs, thus ignoring the linear region, and second the third-order polynomial is not able to properly model the actual tanh-type IV-curve of the differential pair. Therefore, the result in Eq. 4.9 is valid only in the case of small oscillation swing, when both transistors remain in saturation. Indeed, simulations show $\sqrt{I_{bias}}$ -type dependency prior to the linear dependency region. However, to design an oscillator to operate at a small oscillation swing is not a good design choice, and therefore this analysis is of minor practical interest.

4.2 Bias Arrangements

Although the basic cross-coupled NMOS pair is a very simple circuit and easy to design, the proper selection of the bias arrangement is a tricky question. According to the small-signal analysis, the type of bias source has no effect, since it is behind a virtual ground. As we will see the bias arrangement has a significant impact on the oscillator operation, and this once again emphasizes the limitations of the small-signal analysis. The requirements of sufficient transconductance for the oscillation start-up and the estimation of the oscillation amplitude are fairly simple matters, leaving phase noise as the main concern. Since phase noise-related issues often dominate design choices, at this point it is worthwhile to summarize the main processes for the phase noise generation, although some issues have already been discussed. Several noise conversion mechanisms, as well as several noise sources, exist, and the impact of each mechanism and source varies, depending on the circuit topology and the even device dimensioning. Thermal noise (HF noise) and 1/f noise (LF noise) have different conversion paths to phase noise. Furthermore, nonlinear capacitors play an essential role, and the amounts of these vary in different circuits. For these reasons it is not possible to identify a single dominant noise mechanism. For the basic circuit depicted in Figure 4.1 we may consider at least the following noise-to-phase noise conversion mechanisms:

1) Mixing: thermal noise at $2f_{osc}$ is converted into phase noise by the switching of the CCP [4.7],[4.8].
2) The phase noise contribution of the main transistors is independent of their g_m [4.8].
3) AM - FM: the LF noise of the bias source modulates the oscillation amplitude, and this is transformed to phase noise by the nonlinear capacitors in varactors [4.9], [4.10], and also in the active devices [4.11].
4) Common mode - FM: the DC level of the oscillation waveform is modulated by the LF noise of the bias source, and the average value over each period is not constant. Nonlinear capacitors referring to this voltage are upset, resulting in phase noise [4.9].
5) Groszkowski effect: the nonlinearity of the CCP, and thus the oscillation waveform distortion, is a function of the bias current. LF noise is converted into phase noise via this mechanism [4.8].
6) Tail capacitance modulation: the LF noise of the CCP devices creates a fluctuating offset voltage that unbalances the differential pair inducing a noisy current into the capacitance seen at the common-source node (C_{tail}). This current mixes down to the f_{osc} and finally converts into phase noise [4.8],[4.12].

Figure 4.3 depicts several bias arrangements, and we will now compare them, first by pondering the behavior of the circuit and then by performing simulations.

In Case (a) the sources of the NMOS devices are directly connected to ground, and there is no separate element to set the bias current. The transistors are biased to a high bias point V_{DD}-V_{TH} and therefore small devices are sufficient resulting in a wide tuning range in VCO applications. On the other hand, as a result of the high bias point the devices are operating in the linear region for a significant portion of the oscillation cycle, and they load the resonator. In other words, both transistors are open simultaneously for a fraction of the cycle, and here the non-active transistor provides a low-impedance path to ground. We can consider this as a degradation of the resonator Q-value. Furthermore, this arrangement is prone to process spread, and there is no method for any post-tuning. Since now the bias current and device size are bound together, we have limited design freedom. In practice the device size must be selected to be such that the oscillator operates in the voltage-saturation mode. In the comparison tables 4.1 and 4.2 this case shows actually a good performance. For tolerating the process spread larger devices should be used in real design, and the performance would be worse.

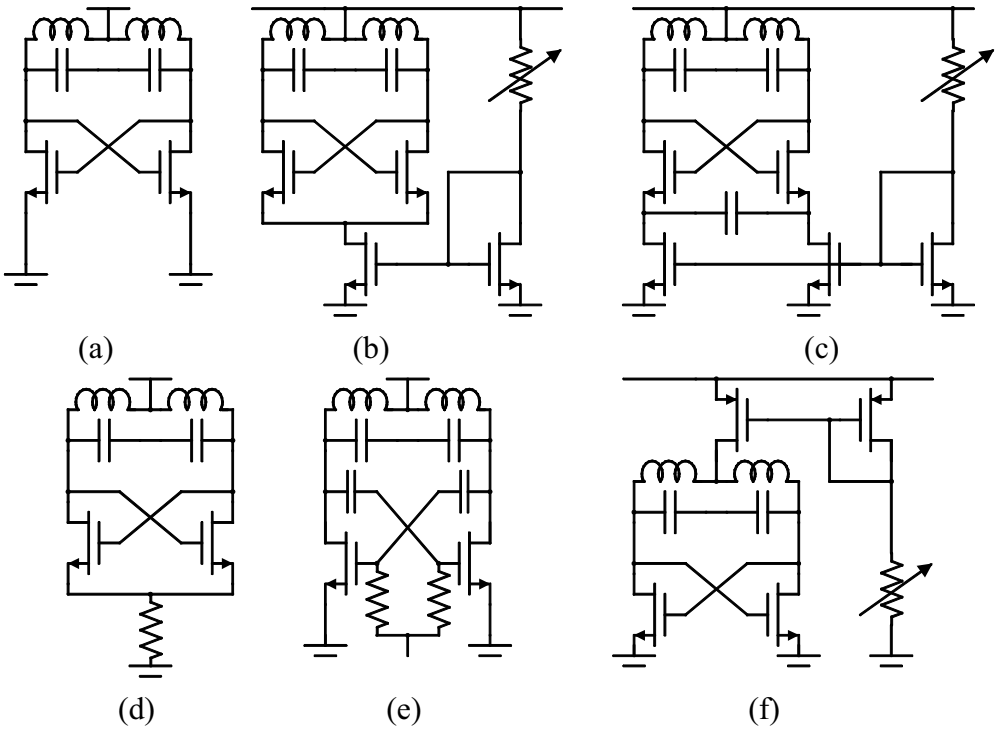


Figure 4.3. NMOS CCP oscillators with different bias arrangements. The bias-current tuning is depicted with a tunable resistor to emphasize that it is also a source of noise.

Using a current sink can solve most of the problems of the previous case. This type of tail-biased circuit is depicted in Case (b) in Figure 4.3. The current sink is used to set the bias current and the CCP transistors can be sized to a low bias point (V_{GS}-V_{TH} value) for a good performance. Compared to Case (a), the CCP transistors switch state more rapidly, and therefore they are open simultaneously for a shorter time. Furthermore, the opposite transistor does not have a low-impedance path to ground. These issues prevent the degradation of the resonator Q-value. The current sink provides a method to compensate for process spread and for power management. The penalty of this arrangement is that now the current sink becomes a significant contributor to phase noise. In addition, at a large oscillation amplitude the current sink is eventually driven out of saturation, resulting in higher phase noise. This limits the acceptable oscillation amplitude. The design of the current sink therefore has a significant impact on the performance of the oscillator. Large device length offers lower noise, higher output conductance and smaller g_m. At very large values the parasitic capacitance becomes so large that it provides a low-impedance path to ground, resulting in the degradation of the resonator Q-value. A small current mirror ratio reduces the impact of the bias generator noise, but at the same time impairs power efficiency.

Case (c) shows one re-arrangement of Case (b). Decoupling the sources of the CCP with a capacitor eliminates the fluctuations of the second harmonic in the common-source node, and therefore suppresses noise up-conversion. If the capacitor is a small one, it acts as a capacitive source degeneration device. Then the parasitic capacitance of the CCP is smaller, and thus the oscillation frequency is higher. Unfortunately, the oscillation amplitude is also lower and the phase noise higher. A larger source-coupling capacitor acts as a short circuit at the oscillation frequency. However, a quite small value (0.6pF in simulation for Table 4.1) is sufficient. This arrangement shows a slight improvement on the previous case.

In Case (d) the current sink is replaced by a resistor to avoid flicker noise. Compared to Case (a), we now have a lower loading of the resonator, and we have some freedom in choosing the

active device bias point. If needed, coarse bias current tuning is also possible with a switched resistor network. Compared to Case (b), no power is wasted in the bias chain and less noise is generated.

Case (e) solves the biasing issue by using additional blocking capacitors. The bias point and thus the device sizes can now be set for a good performance. A very low bias point results in devices operating in the switch-type mode. The circuit has good power efficiency but the oscillation waveform tends to be non-symmetric and the close-in phase noise is a little higher than in the basic Case (a). Blocking capacitors may occupy a large die area and suffer from parasitic capacitance. Moreover, high-value bias resistors are needed to avoid the loading of the resonator, and therefore they consume die area.

In Case (f) the current sink of Case (b) is replaced by a PMOS current source. The PMOS device is built in an N-well, and thus has less substrate noise pick-up than its counterpart in the basic CMOS technology. Furthermore, in some technologies PMOS devices have lower noise than NMOS devices. Other benefits are that the output DC level is better suited for driving the output buffers and the oscillation voltage swing remains below the supply level.

The six circuits depicted in Figure 4.3 were simulated using the same resonator to gather some insights into this matter. The results are given in Table 4.1. The targeted performance and resonator structure are chosen to be comparable to the previous Colpitts oscillator simulations presented in Table 3.5. Since noise up-conversion is strongly related to nonlinear capacitors, a second set of simulation results is given in Table 4.2. The linear capacitor is replaced by a tunable capacitor of corresponding size, which is a high-Q inversion-mode NMOS device. See Section 6.4 for further details on the MOS-varactor. The tuning range is given in percentages in the comparison table. It is defined by TR%= absolute tuning range / center frequency. The oscillation amplitude depends on the L/C ratio (Eq. 3.37), and hence the oscillation amplitude varies a little (200-300 mV_{pp}) within the tuning. Moreover, phase noise and the main source for it vary considerably within the tuning range. For example, for Case (d) the lowest phase noise $\mathcal{L}$(1MHz)=-126 dBc/Hz is achieved at the lower end of the tuning voltage range, and phase noise is mainly due to thermal noise. The worst value $\mathcal{L}$(1MHz)=-121 dBc/Hz appears at maximum tuning voltage, and now the LF noise originating from the main transistors is the greatest contributor. The simulation results show that actually a very simple resistor biasing gives the best performance. One of the big questions here is the process variation. If the device characteristics have large deviations, then we need aggressive post-tuning, and simple resistor biasing is not sufficient. However, the resistor biasing can also be tuned with a switched network [4.12]. The fact that the optimum choice of the circuit topology depends on the technology and on the targeted performance, particularly on the frequency tuning range and the mechanism used for achieving it, makes a precise and undisputed comparison problematic.

Table 4.1. Properties of oscillators in Figure 4.3. L=2nH/2Ω, C=1.3pF, V_{dd}=1.2V

Case	Freq [MHz]	$V_{osc,SE}$ [V_{pp}]	I_{DC} [mA]	$\mathcal{L}$(10kHz) [dBc/Hz]	$\mathcal{L}$(1MHz) [dBc/Hz]	Pushing [MHz/V]	1/f corner [kHz]	C_{par} [fF]	FOM [dB]
(a)	3100	1.9	2.6	-79	-126	1	50	16	191
(b)	3040	1.9	2.7	-67	-124	22	800	73	189
(c)	3050	1.9	2.7	-74	-125	6	250	60	190
(d)	3070	1.9	2.3	-84	-127	2	20	43	192
(e)	3090	1.9	1.8	-78	-128	1	200	27	194
(f)	3040	1.8	2.7	-65	-123	21	900	75	187

Pushing is simulated with values V_{dd} / V_{dd}+10mV, $C_{par}=(L\omega^2)^{-1}$-C

Table 4.2. The same circuits with the same component values as in Table 4.1, but now the linear capacitor is replaced by an NMOS-varactor. The worst value within the tuning range is given.

Case	Freq [MHz]	TR%	$V_{osc,SE}$ [V_{pp}]	I_{DC} [mA]	$\mathcal{L}$(10kHz) [dBc/Hz]	$\mathcal{L}$(1MHz) [dBc/Hz]	FOM [dB]
(a)	2830-3300	15	1.5	3.0	-61	-118	182
(b)	2780-3220	14	1.6	2.9	-59	-117	181
(c)	2800-3230	14	1.6	2.8	-61	-118	183
(d)	2800-3260	15	1.6	2.5	-63	-121	185
(e)[1]	2840-3250	14	1.9	4.3	-71	-122	185
(f)[2]	2880-3280	13	1.2	3.0	-48	-108	172

1) Bias point changed from 0.5 to 1.2 V
2) Additional RC biasing is used for the MOS-varactors in Case (f).

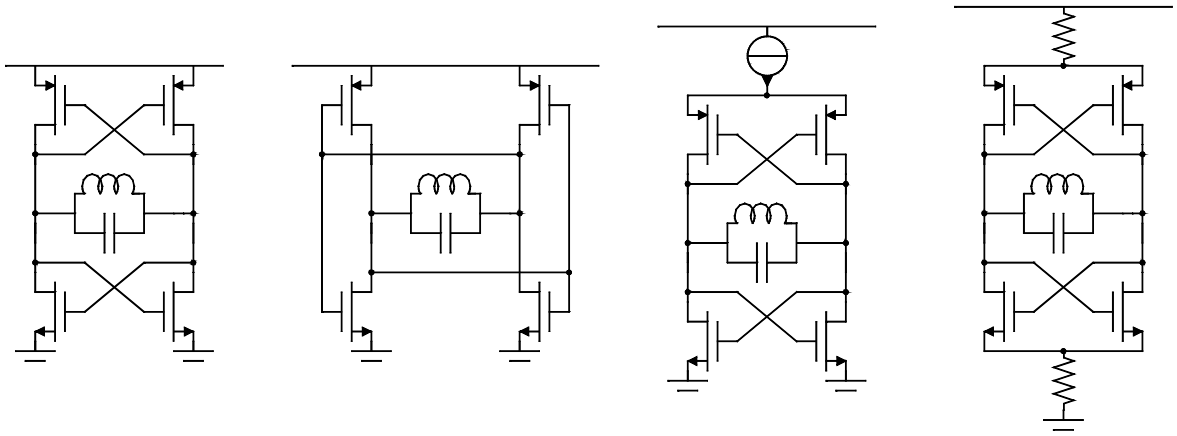
In addition to the presented biasing schemes, there are many with a slightly higher complexity, such as adding a large tail capacitor [4.13], adding a series resistor to the current source [4.14], RC filtering in the current mirror [4.15], a cascade current source [4.16], a source follower-type current source [4.17], the use of a "memory reduction tail transistor"[4.18], a parasitic lateral NPN transistor as a current source [4.19], source degeneration of the current source [4.20], and a pulsed tail current [4.21]. Cases (e) and (d) were combined in [4.22], and combinations of Cases (e) and (b) with an additional tail transistor appear in [4.23],[4.24]. In the current-sink biased circuits high-frequency noise at $2f_{osc}$ and the fluctuation of the potential of the common-source node are strong noise contributors. An LC filter resonating at $2f_{osc}$ can be used to suppress these effects [4.25]-[4.30]. LC filters are used to either push up or diminish the impedance of the common-source node at $2f_{osc}$. Since the capacitance is often quite small, the inductor becomes relatively large. This LC-filter technique expands the die area considerably, and although efficient, it is therefore not a very attractive approach.

4.3 PMOS and CMOS Circuits

A p-type MOSFET is a complementary device to the NMOSFET, and we can convert any NMOS circuit to the corresponding PMOS circuit. So, for instance, all the circuits depicted in Figure 4.3 have an equivalent PMOS version. Although the charge carrier mobility is lower in the p-type devices, in modern CMOS technology the p-type devices also have sufficient performance for RF applications. PMOS devices are larger for the same g_m as their counterparts, and hence they suffer from lower g_m/i_{bias} and larger parasitic capacitance. Furthermore, the threshold voltage is not exactly opposite. In modern CMOS technologies the PMOS/NMOS size ratio is about 2½ for the basic inverter stage. In a basic CMOS technology PMOSFETs are built in an N-well, and thus have some isolation from the substrate. Some authors claim that since the intrinsic noise of the PMOS devices is lower, a PMOS-only oscillators would be the optimal solution [4.31],[4.32],[4.33]. However, in some technologies even the noise level is not lower [4.34], an observation which I have also made for one 65-nm CMOS technology. Furthermore, since the PMOS devices are larger, these oscillators suffer from narrower tuning range, and if this is compensated during the design procedure, the eventual circuit will not necessarily show a better performance. The use of PMOS-only topology instead of an NMOS-only topology needs detailed study with the given technology and performance targets. Personally, I have not found them better in the cases I have been involved in.

In CMOS cross-coupled pair circuits both PMOS and NMOS pairs are used simultaneously. Some arrangements are depicted in Figure 4.4. We may consider CMOS CCPs as a current

reuse technique. On the other hand, we may consider that simple CMOS inverters are now used as oscillating amplifiers. Since the bias current is used twice, we have a higher amount of transconductance ($g_{m,tot} = g_{m,NMOS} + g_{m,PMOS}$), and for the same current the oscillation amplitude is twice that found in an NMOS or PMOS-only circuit [4.13], assuming that operation remains in the current-limited region. A higher transconductance for a given bias current results in faster switching of the CCPs. A CMOS pair has a little more design freedom and we may target a highly symmetrical waveform, which results in a lower 1/f noise corner [4.13]. On the other hand, since active devices separate the resonator from both rails, the CMOS CCP oscillator enters the voltage-limited region earlier than a single-CCP circuit. Therefore, CMOS CCPs offer higher power efficiency and lower phase noise for a given current, but ultimately the lowest phase noise is achieved with a single-CCP topology.



(a) (b) (c) (d)

Figure 4.4. Some CMOS cross-coupled pair oscillator circuits.

For the optimum sizing of the NMOS and PMOS pairs for a CMOS CCP circuit, we need to perform a detailed circuit design. Simple rules, such as $g_{m,NMOS}=g_{m,PMOS} \rightarrow W_{PMOS}=(\mu_N/\mu_P)\cdot W_{NMOS}$ [4.35], fail to predict the optimum performance. Hajimiri's ISF theory states that a symmetric waveform gives the lowest phase noise, and this is the main guideline for optimum device sizing. Unfortunately, the nonlinear capacitors in the resonator also impact on the symmetry, and therefore a simple rule for the W_{PMOS}/W_{NMOS} ratio is not available. Furthermore, the large parasitic capacitance from the resonator nodes to ground results in an increased noise contribution of the PMOS pair [4.36]. In such a case we need to compensate for this by reducing the size of the PMOS pair, and the optimum W_{PMOS}/W_{NMOS} differs from that of the small parasitic capacitance case. In addition, the process spread needs attention. In single-CCP circuits the initial bias point is always correctly set, whereas for CMOS cases it may occur that the bias point is shifted. A common-mode feedback circuit can be used to set the initial bias point to a proper value, but this may have a noise penalty, although with proper design such feedback can even be used for noise filtering [4.37]. Concerning bias arrangements in general, one may repeat a similar type of bias structure comparison for the CMOS CCP as we did for the NMOS CCP, but now it is even more extensive, since the CMOS CCP circuit can be biased from the tail or from the top, or both common-source nodes can be manipulated. Such discussion will not be repeated here, since the trends and results are similar to what we learnt in the NMOS case.

The detailed comparison of all existing cross-coupled NMOS/PMOS/CMOS oscillator circuit variants would be an enormous task, since the number of circuits is large, the frequency-tuning elements, as a part of the resonator, impact on the comparison, and different technologies have their own impact as well. To keep this comparison to a reasonable length, I have selected a set

of eight circuits all simulated in the same 0.13-μm CMOS technology. The simulation results are summarized in Table 4.3. Only a linear resonator case is studied here, once again to keep the discussion brief. The best varactor arrangement depends on the circuit as well, and to take this into account would make this discussion messy.

Table 4.3. Properties of some CCP oscillators. Resonator: L=4nH/4Ω, C=0.65pF, V_{dd}=1.2V

Circuit	Freq [MHz]	$V_{osc,SE}$ [V_{pp}]	I_{DC} [mA]	ℒ(10kHz) [dBc/Hz]	ℒ(1MHz) [dBc/Hz]	FOM [dB]
NMOS CCP, R bias Fig. 4.3(d)	3072	1.9	2.3	-84	-127	192
PMOS CCP, R bias Counterpart of above	3040	1.8	2.4	-83	-127	192
CMOS CCP, R bias Fig. 4.4(d)	3060	0.8	0.4	-71	-122	195
NMOS CCP, [4.25] NMOS bias with LC filter	3040	2.0	2.5	-85	-133	198
PMOS CCP, PMOS bias with LC filter	3000	1.7	2.5	-85	-132	196
CMOS CCP, PMOS bias with LC filter	3050	0.8	0.5	-80	-122	194
"Class-C" NMOS CCP [4.23],[4.24]	3030	1.5	1.5	-85	-129	196
"Class-C" PMOS CCP Counterpart of above	3050	1.0	1.2	-82	-126	194

As a summary of the discussion of various cross-coupled pair NMOS/PMOS/CMOS structures, we draw the following conclusions:

- NMOS CCP offers the lowest phase noise.
- CMOS CCP offers the best power efficiency.
- The bias arrangement has a major impact on phase noise properties, in contrast to what simple models, such as Leeson's model, predict.
- Device noise transforms into phase noise via multiple mechanisms, and detailed simulations are therefore necessary. Simple design formulas are not sufficient.
- No clear winner exists among the various circuit arrangements.

4.4 BJT Specific Issues

The fact that in bipolar transistor (BJT) circuits the base-emitter junction has almost constant voltage over it in the active operating mode (V_{BE} ~0.7-0.8V) limits the circuit arrangements, though it also makes the DC biasing of BJT circuits simple and reliable. It also limits the usefulness of BJTs in low-voltage applications. The basic npn-CCP, depicted in Figure 4.5a, is biased to V_{CE}=V_{BE}, and V_{BC}=0V. Therefore the oscillation amplitude is limited and the oscillator enters the voltage-limited region a little earlier than $V_{osc,pp}$=V_{BE}. As such, the oscillation amplitude and phase noise vs. bias current characteristics are very similar to what was previously found for other oscillators, see at Figure 3.16. Achieving a higher oscillation amplitude calls for methods to set the collector-emitter bias higher. In the absence of good (low parasitics) by-pass capacitors, the cross-coupling must be implemented with emitter followers. This is depicted in Figure 4.5b. Now V_{CE}=2V_{BE}, and V_{BC}=- V_{BE}. If good by-pass capacitors are available we may use diodes and small by-pass capacitors instead of voltage-followers, as shown in Figure 4.5c. As the BJT and SiGE HBT technologies evolved in the late 1990s and

the understanding of noise issues improved, it became a prevalent praxis to use RC biasing, shown in Figure 4.5d, for npn-CCPs [4.38]-[4.46]. This method enables the bias to be set for optimum performance. This circuit arrangement is almost the same as the "Class-C" CMOS oscillator [4.23,4.24], although it is derived from a different basis.

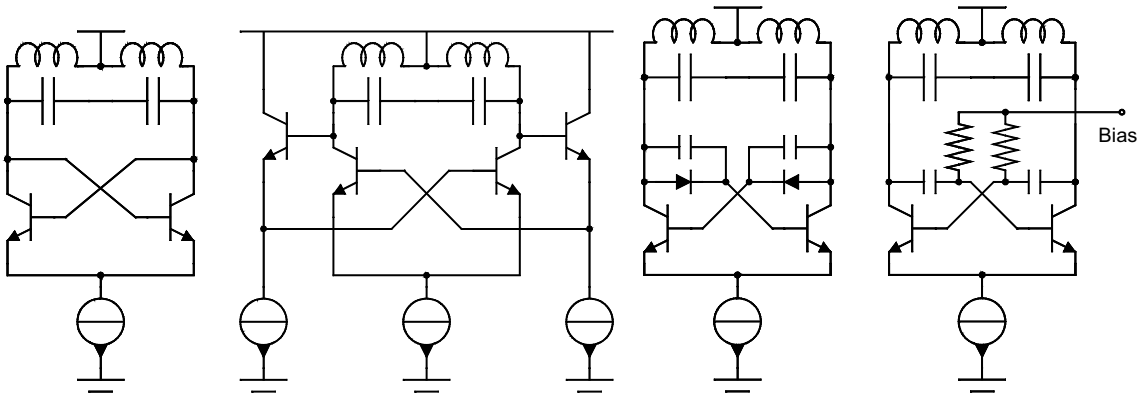


Figure 4.5. Some npn BJT CCP oscillators.

Table 4.4. Properties of the npn-CCP oscillators shown in Figure 4.5. Resonator: L=2nH/2Ω, C=0.65pF, V_{cc}=2V, the active device is a double-base SiGe HBT. An npn current mirror is used for biasing.

Circuit	Freq [MHz]	$V_{osc,SE}$ [V_{pp}]	I_{DC} [mA]	$\mathcal{L}$(10kHz) [dBc/Hz]	$\mathcal{L}$(1MHz) [dBc/Hz]	FOM [dB]
Basic npn-CCP, V_{cc}=1.2V Fig. 4.5(a)	2890	0.7	0.9	-78	-118	187
Same as above Active device 4x bigger	2400	0.7	1.3	-80	-121	186
npn-CCP with emitter follower, Fig. 4.5(b)	2950	1.4	3.2	-79	-121	183
npn-CCP with diodes, Fig. 4.5(c)	2890	1.1	1.4	-81	-121	186
npn-CCP with RC bias Fig. 4.5(d)	2950	1.3	1.5	-80	-122	187

A specific issue when considering BJT oscillators is the base resistance. The impact of the gate resistance in MOSFET oscillators was already briefly emphasized. In the case of the BJT oscillators the base resistance is far larger, and it is often the strongest noise source. As an example, the base resistance for the transistor used in the simulations in Table 4.4 is 52 Ω, while the gate resistance for the MOS devices used in the simulations in Table 4.3 is about 10 Ω. The base resistance can be reduced by using a larger device, or in practice, several devices in parallel. The penalty is increased parasitic capacitance, and hence we once again meet the phase noise – tuning range trade-off. In fact, even if the BJTs have a higher transconductance per unit current and lower flicker noise corner than the MOSFETs, the finite base resistance severely limits the performance and therefore in a BiCMOS process an NMOS CCP will most probably be superior to a BJT CCP. Here it is worthwhile to emphasize that large base resistance is not as a severe problem for discrete transistors, where the fabrication process and device structure can be optimized for a low base resistance.

Once again, to gain some insight into this topic, we will make a small comparison of these BJT oscillators. We use the same linear resonator as previously, and the active device is a double-base SiGe HBT from a 0.9-μm process [4.47]. The simulation results for the four oscillators depicted in Figure 4.5 are given in Table 4.4. In addition, the second row shows the impact of increased active device size on reducing the base resistance. The first circuit, the basic CCP, is simulated with a supply of 1.2 V since it does not favor a higher supply, while the rest of the circuits need a higher supply, and 2 V is used here.

4.5 Unity Feedback vs. Reactive Feedback

During the era of discrete transistors reactive feedback oscillators, such as the Colpitts oscillator, were favored. This is partly explained by the technological issues and partly by tradition. No hard evidence for the superiority of the Colpitts oscillator over other arrangements was given. The simple analysis carried out in this thesis shows that in the Colpitts oscillator a higher initial gain is needed compared to unity feedback arrangements. Furthermore, in the Colpitts oscillator the selection of the capacitance ratio poses a trade-off between the tuning range and the required transconductance. The comparison tables that are presented also indicate that cross-coupled pair oscillators have a better performance. Andreani et al. use the ISF theory to compare the Colpitts and CCP oscillators in [4.48]. They conclude that the CCP oscillator is superior to the Colpitts oscillator. Personally, each time I have faced a new IC technology in project work I have repeated a simulation-based comparison of various oscillator candidates, including Colpitts, Hartley, and many CCP circuits. I have not observed that reactive feedback circuits would provide better performance than the CCP circuits, at least not under the restrictions of monolithic implementation. I am convinced that tens or even hundreds of IC engineers have made the same types of comparisons. The popularity of the CCP structures compared to the reactive feedback circuits indirectly proves the superiority of the unity-feedback structures for RF IC applications. However, one needs to be enthusiastically open to all kinds of new ideas, and continue these comparisons and studies, since there is a dangerous tendency in science and in engineering to fall into a mode of stagnant doctrine.

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5 Monolithic Inductors

Monolithic inductors are an essential part of modern RF IC design. They find their use in LC-oscillators and filters, in matching and feedback circuits, and as a load element in amplifiers and mixers. It is crucial for smooth and successful design flow that accurate inductor models are available. Unfortunately, despite the recent high level of activity in this field, foundry-supported inductor models are not a self-evident matter. In GaAs foundries the primary target applications are RF and microwave circuits and already in the early 1990s scalable inductor models were generally available [5.1]-[5.4]. In silicon technologies, prior to the "GHz-era", inductors were considered impractical. Some papers in the early 1990s [5.5]-[5.14] demonstrated the potential and, in conjunction with the increased operating frequency and telecommunication boom, led to high levels of research activity. The present status is that some foundries, particularly the ones dedicated to RF ICs, do provide good models, while the rest provide preliminary-level material or no models at all. In most foundry models a problem is that they are for a fixed geometry and do not allow any variation in this respect. Furthermore, these models, such like any device models, have a limited range of validity, and they may include mistakes, as well as conceptual errors. For these reasons it is highly recommended that RF circuit designers are aware of various detailed issues concerning monolithic inductors and are able to verify given models, as well as develop their own ones.

There are four methods of model development:

1) Analytical and semi-empirical equations can give estimations of inductance value and losses. They are not accurate enough for actual device modeling. However, they are useful for gaining an understanding of device performance.
2) A small set of inductors is fabricated and measured. The resulting inductor library can be used for preliminary-level circuit design. However, a fixed set of inductance values limits the circuit design and, second, the inductors are not optimal for a given circuit.
3) An extension of the previous case is to fabricate a large set of inductors and to provide these as an inductor library or to develop a scalable model based on these devices. This method is generally used in the development of a foundry library. This method is adequate, but has some problems: the inductor geometry is still fixed and a scalable model may include some inaccuracies. Foundries supporting a scalable model unfortunately do not usually provide device s-parameters, which could be used as an accurate model in the final circuit simulations.
4) The use of an electro-magnetic (EM) field simulator: this method allows full freedom in the geometrical structuring and gives the opportunity to optimize an inductor for a given task. There are, however, major weaknesses: the correct use of EM-simulators is not obvious and the simulation results must be verified to measured devices. In addition, it is a tedious task to simulate a large number of inductors. Despite involving a lot of work, this method is the best way for device optimization, at least when there is no opportunity to a large-scale work proposed in Case 3 above.

For the oscillator applications, the main target in inductor development is to create an inductor with the desired inductance-value and the lowest loss and parasitic capacitance. One typical target is to maximize the quality factor at a given frequency. However, this may lead to unacceptable parasitic capacitance and die area, resulting in a trade-off situation. Often, a completely opposite situation may exist and the target is then to minimize the die area that is occupied by an inductor with reasonable characteristics. If an inductor is used as a load element in an amplifier, we want to maximize the equivalent parallel resistance R_p of the inductor. The quality factor for a parallel L-C-R_p network with an ideal capacitor can be expressed as

$$Q = \frac{R_p}{\omega L} \quad \Rightarrow \quad R_p = Q\omega L \tag{5.1}$$

Therefore, the product of Q and L must be maximized for the highest gain at the frequency of interest. The process characteristics, such as the number of metal layers, the conductivity of each metal layer, and the substrate losses, have a strong influence on the inductor characteristics, and therefore it is not possible to make general process-independent optimization rules. Instead, each process requires its own study.

This chapter is organized as follows. After a brief discussion of quality factor definitions, the structural matters and loss mechanisms are discussed. Then equivalent circuits and parameter extraction procedures are studied. Analytical, semi-empirical and scalable models are presented in Section 5.4. Then electro-magnetic field simulations are discussed and an automated simulation environment is reported. Finally, there is some discussion about the use of bonding wires. I have intentionally omitted any discussion about non-standard fabrication techniques and monolithic transformers.

5.1 Quality Factor

Until now, I have used the term quality factor Q as a general concept for losses in a reactive component. Some confusion exists in the literature concerning the definition of Q, and therefore more detailed discussion is justified.

The most general definition of the Q-factor is based on the ratio of stored energy to dissipated energy per cycle:

$$Q = \frac{E_{store}}{E_{diss} / \omega} \tag{5.2}$$

For an ideal inductor with a series resistor R, we have

$$Q = \omega \frac{\frac{1}{2}Li^2}{\frac{1}{2}Ri^2} = \frac{\omega L}{R} \tag{5.3}$$

This simple calculation method becomes complicated when we have a more generalized circuit. An alternative method is to consider the 3-dB bandwidth of a resonator:

$$Q_{3dB} = \frac{\omega_0}{\Delta\omega_{3dB}} \tag{5.4}$$

Furthermore, the quality factor can be related to the phase response and calculated with [5.15]

$$Q_\phi = \frac{\omega_0}{2}\left|\frac{d\phi}{d\omega}\right| \tag{5.5}$$

where ω_0 is the resonance frequency and the phase derivative is also calculated at the resonance frequency. For an inductive one-port, this equals

$$Q_\phi = -\frac{\omega_0}{2}\frac{d}{d\omega}\left(\arctan\left(\frac{\mathrm{Im}(y_{11})}{\mathrm{Re}(y_{11})}\right)\right)_{\omega=\omega_0} \tag{5.6}$$

In numerous papers the following definition for the Q-factor of a one-port is used:

$$Q_{11} = \frac{\left|\mathrm{Im}\left\{Z_{in}\right\}\right|}{\mathrm{Re}\left\{Z_{in}\right\}} = \frac{\left|\mathrm{Im}\left\{Y_{in}\right\}\right|}{\mathrm{Re}\left\{Y_{in}\right\}} = \frac{\left|\mathrm{Im}\left\{y_{11}\right\}\right|}{\mathrm{Re}\left\{y_{11}\right\}} \tag{5.7}$$

For a simple LR-circuit this definition leads to the same result as our initial definition. However, at the self-resonance frequency of a parallel LC-resonator $Q_{11}=0$, whereas it actually has a finite quality factor just like any resonator. The wide use of the Q_{11} definition in the literature leads to some misconceptions, since it indicates a roll-off of the Q-factor by the definition itself. In reality, the same kind of roll-off does exist, but it is inextricable from that caused by the Q_{11} definition. This issue is also discussed in [5.16]-[5.19].

In order to gain some practical insight into this matter, let us study two cases. In the first case an ideal LCR-circuit is studied and in the second one a real monolithic inductor in used. The Q-factor in the Q_{11} sense for a parallel LC-resonator with a series resistance in the inductor can be expressed as

$$Q_{11} = \frac{\omega^3 L^2 C + \omega(CR^2 - L)}{R} \tag{5.8}$$

This kind of Q-value has a zero at the self-resonance frequency

$$\omega_{SR} = \sqrt{\frac{1 - CR^2/L}{LC}} \tag{5.9}$$

and the maximum Q-value is achieved at a frequency where $dQ_{11}/d\omega=0$.

$$\omega_{Q11,\max} = \sqrt{\frac{1 - CR^2/L}{3LC}} = \frac{1}{\sqrt{3}}\,\omega_{SR} \approx 0.6\,\omega_{SR} \tag{5.10}$$

If the Q_{11}-plot has a Q-maximum far before this value, it indicates that frequency-dependent losses have a significant impact on that particular device. This is a somewhat poor illustrative method to present losses, although it works in practice: inductors are generally used at a frequency range where this Q_{11} maximum appears.

To be able to derive the Q_{3dB} and Q_ϕ plots, an ideal capacitor is connected in parallel with the device under test. The value of this capacitor is then swept and the Q-values are calculated at each resonance frequency ω_c. For our ideal LCR-circuit under study, the quality factor is given by

$$Q = \frac{L}{R}\omega_c \tag{5.11}$$

Thus, any frequency dependency is caused either by the inductance or resistance variations. Since the appropriate amount of capacitance is set in parallel with a possible parasitic capacitance in a real inductor, it has no effect on this matter.

Figure 5.1 depicts the frequency response of the various Q-definitions for the LCR-circuit being studied and Figure 5.2 shows the same study for a real 4.7-nH inductor fabricated in the *Mietec C05M* CMOS process. By comparing these figures we can note that the maximum of Q_{11} has shifted to a lower frequency. Both the Q_{3dB} and Q_ϕ curves are almost identical, and in general they do give roughly equal results.

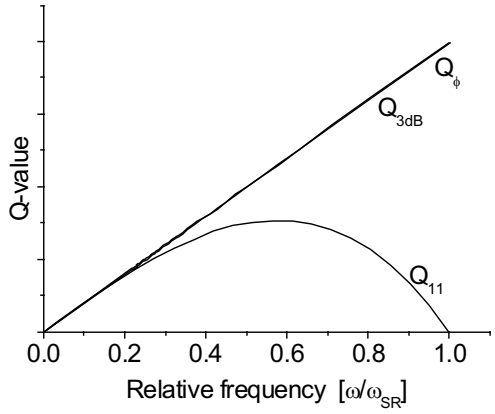

Figure 5.1. Various Q-definitions for an ideal LCR-circuit.

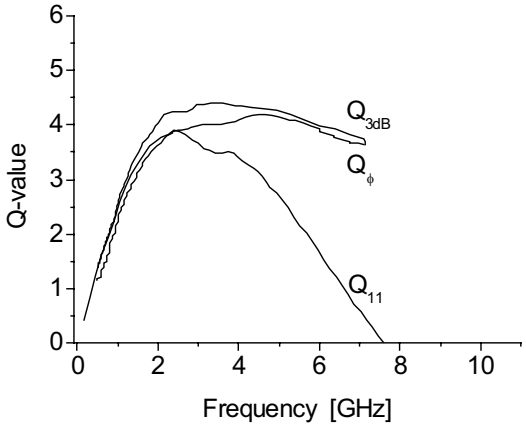

Figure 5.2. Q-values for a real monolithic inductor on a silicon substrate.

5.2 Structures and Loss Mechanisms

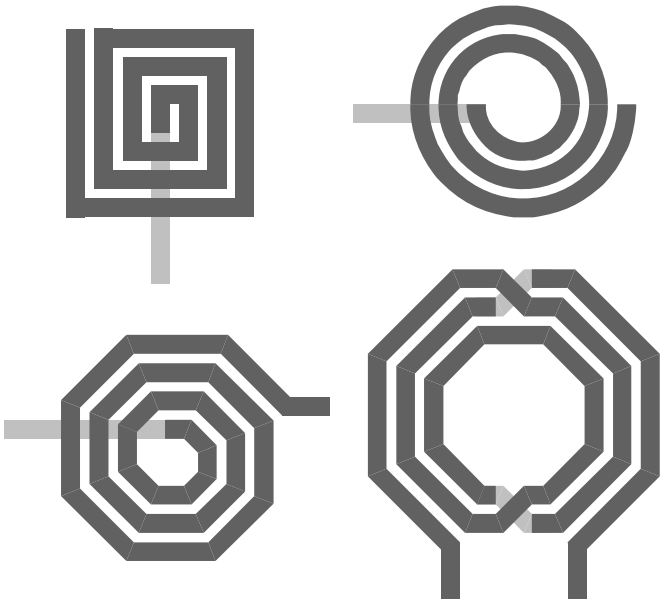

Figure 5.3. The most common geometrical shapes for monolithic inductors: square, circular, and octagonal. In the lower right-hand corner a symmetrical octagonal structure is presented.

The most common geometrical structures for planar inductors are illustrated in Figure 5.3. A square inductor has the best inductance vs. die area ratio, but it performs poorly at high frequencies. On the other hand, a circular inductor wastes die area, but the high-frequency losses are smaller thanks to the lack of corners. An octagonal inductor is a compromise between these two. Many foundries do not allow curved shapes, and thus an octagonal structure is preferred. All these structures can be drawn in a symmetrical fashion as well. The dimensions are defined using the width of the strip (W), spacing between adjacent strips (S), the amount of empty space in the middle (D_{in}), and the number of turns (NT). It is possible to vary the spacing and width in consecutive turns in order to slightly improve the characteristics. Furthermore, several metal layers can be combined in various fashions.

5.2.1 Conductor Losses

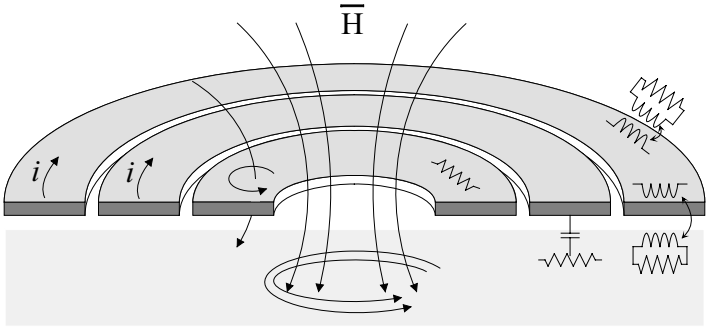

Figure 5.4. Eddy currents in a conductor strip and in the substrate are illustrated in the left-hand part of the figure. On the right, the lumped elements depict resistive losses in the conductor, capacitive and magnetic coupling to a lossy substrate, and losses in the conductor strip caused by the eddy currents.

DC resistance, the skin effect, and current crowding effects cause losses in a conductor strip. The DC resistance is related to the length of the metal line vs. its cross-section and conductivity:

$$R_{DC} = \frac{l}{Wt\sigma} \tag{5.12}$$

At high frequencies the EM fields penetrate only into a fraction of the cross-section of a conductor. The depth at which the fields decrease to 1/e is called the skin depth and is given by [5.20]

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}} \tag{5.13}$$

Now the resistance at high frequencies is [5.21]

$$R_{rf} = \frac{l}{W\delta(1-e^{-t/\delta})\sigma} \tag{5.14}$$

The resistance of thick (t>>δ) wire can be approximated with

$$R = \frac{l}{W\delta\sigma} = \frac{l}{W}\sqrt{\frac{\pi\mu}{\sigma}}\sqrt{f} \tag{5.15}$$

Thus, the skin effect is dependent on the square root of the frequency. In practice, a scaling factor f_{sk} is used for this effect and losses are expressed as

$$R = R_{DC}\left(1+\sqrt{\frac{f}{f_{sk}}}\right) \quad or \quad R = R_{DC}\sqrt[4]{1+\left(\frac{f}{f_{sk}}\right)^2} \tag{5.16}$$

In Figure 5.4 the magnetic flow H and an eddy current induced into the adjacent trace are depicted. These eddy currents add to the excitation current of the inductor on the inside edge and subtract it from the outside edge [5.22]-[5.24]. Thus, the resulting non-uniform current flow increases the effective resistance. This current crowding effect is studied analytically in [5.23] and the authors suggest that the effective resistance can be expressed as

$$R_{crow} = \frac{R_{DC}}{10}\left(\frac{f}{f_{crit}}\right)^2 \quad where\ f_{crit} \approx const \cdot \frac{R_{sheet}}{W} \tag{5.17}$$

The parameter f_{crit} describes the on-set of this effect. According to the authors, the effect also has a turn-off frequency and it is four to six times f_{crit}. Furthermore, the authors emphasize that the analytical results are "simple rough estimates", since the problem is complex and manifold. Therefore, these results should be considered as guidelines. Current crowding also takes place in the bends of the conductor. Figure 5.5 shows how the current density is higher at the inner edge of each corner. The current crowding effect can be reduced by splitting the trace into narrower parallel strips [5.25], or by using tapering [5.26]-[5.28]. Both of these techniques require an extensive amount of optimization work and yet the improvement in the Q-value remains rather small in most cases. Therefore, these methods are not widely adopted. Instead, it is a prevalent practice to completely omit the innermost turns, resulting in a hollow inductor [5.29]-[5.30]. A good rule of thumb is to have $D_{in} \geq 5 \cdot W$ [5.29]. Eddy currents in the conductor have an influence on the inductance value as well, since the magnetic flux generated by the eddy current is opposite to the main flux. This reduces the net magnetic flux through the inductor and at high frequencies the inductance decreases [5.30].

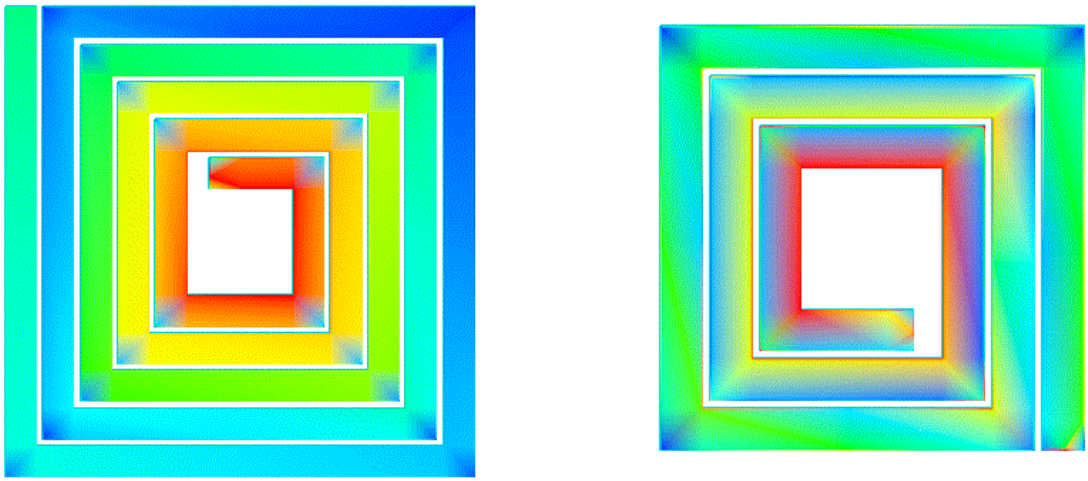

Figure 5.5. Simulated current densities at 5 GHz for two inductors. The current density is illustrated with the "temperature" scale, i.e., red is for high density and blue is for low. On the left the width of the conductor is 10 μm and on the right it is 30 μm. The figures are not to the same scale.

Table 5.1 provides the properties of metals that are commonly used in IC technologies. All these metals have a relative permeability close to one ($\mu \approx \mu_0$). In planar implementation the current flows on both sides of a wide strip and therefore twice the skin depth should be considered. The given values are for pure materials. In IC technologies metals are non-uniform alloys. Therefore, it has been suggested that 80% scaling should be used for conductivity [5.31]. In particular, the conductivity of aluminum is optimistic in the table. In mainstream IC technologies the metal layer thicknesses are typically 1-3 μm and therefore the skin effect is not a significant source of loss at 2 GHz. At higher frequencies or with thick metal its role becomes important. If two metal layers are combined with a continuous via opening the resulting conductor is rather thick and the skin effect starts to play a role. In such a case the DC resistance is lower, but the distance to the substrate is reduced, resulting in a lower ω_{SR} and increased substrate losses. In Figure 5.7 the measurement results of various structures fabricated in the *VTTB8* process are depicted. It can be observed that no major improvement is gained by combining metal 1 and metal 2. *VTTB8* was a somewhat old-fashioned 0.8-μm BiCMOS process from the Technical Research Center of Finland. It has two metal layers and moderate substrate resistivity of 30 Ωcm.

Table 5.1. Properties of some common metals.

Metal	Conductivity [10^7 S/m]	Sheet Resistance[1] [mΩ]	Skin depth @ 2GHz [μm]
Aluminum (Al)	3.8	26	1.8
Gold (Au)	4.3	24	1.7
Copper (Cu)	6.0	16	1.5

Note 1: metal thickness of 1 μm is assumed.

5.2.2 Substrate Losses

Substrate characteristics, given in Table 5.2, have a profound impact on the performance of a monolithic inductor and on the optimal structure. Losses in the substrate are caused by capacitive coupling to a lossy material and by inductively generated eddy currents in the substrate. Three clearly distinct substrate categories exist.

1) Insulating and semi-insulating materials, such as quartz, sapphire and GaAs. These kinds of substrates have very low losses, and in most cases they can be approximated as a lossless dielectric material.
2) Low-doped silicon is used in conventional bipolar and BiCMOS processes, as well as in advanced new CMOS processes.
3) High-doped conductive silicon is used in conventional CMOS processes.

Table 5.2. Characteristics of some common substrates.

Material	Resistivity [Ω·cm]	Permittivity (ε_r)
Quartz (glass)	10^{13}	3.7
GaAs	10^{8}	13.1
High-resistivity Si	10^{4}	11.9
Low-doped Si (BiCMOS)	10^{1}	
High-doped Si (CMOS)	10^{-2}	

Silicon processes come in a large variety. Most bipolar and BiCMOS substrates have a resistivity in the range of 10-50 Ωcm and pure CMOS processes either have the same kind of substrate or they use a highly doped substrate with a resistivity of about 0.01 Ωcm. In silicon technologies the existence of an epitaxial ("epi") layer has an impact on the inductor characteristics. Usually, BiCMOS processes may have a thin epi-layer with low resistivity (<1μm, ~0.1 Ωcm), whereas CMOS processes usually have a thick resistive (>1μm, ~10 Ωcm) epi-layer on top of a highly conductive bulk. Some processes, such as *VTTB8*, do not have an epi-layer, and in some cases a mask is offered to prevent the formation of an epi-layer. In the most recent digital CMOS generations there is a tendency towards higher substrate resistivity.

Both capacitive coupling, i.e., by an electrical field, and inductive coupling, i.e., by a magnetic field, cause losses because of the substrate. Capacitive coupling to the substrate causes currents to flow into a nearby ground, as well as radial currents caused by the potential difference over the inductor segments. Thus, both vertical and lateral currents are induced. A magnetic field generates lateral eddy currents into the substrate, and energy is dissipated into lossy material. Second, eddy currents result in a negative mutual inductance with the actual inductor, and thus, the overall inductance value is reduced. A first-order approximation for these losses is that they are related to the occupied die area [5.32]-[5.34]. For BiCMOS substrates losses resulting from capacitive coupling are severe, but the eddy currents are negligible [5.29],[5.35]. In highly conductive CMOS substrates the capacitance to the substrate is also large since the substrate is almost a ground plane and therefore the self-resonance frequency is severely reduced [5.34].

Substrate induced losses are, to some extent, frequency-dependent, since the substrate skin effect causes the currents that are induced to flow closer to the substrate surface. The skin depth is given by Equation 5.13 and is related to frequency and substrate conductivity. Figure 5.6 compares the characteristics of an inductor on top of three different substrate materials.

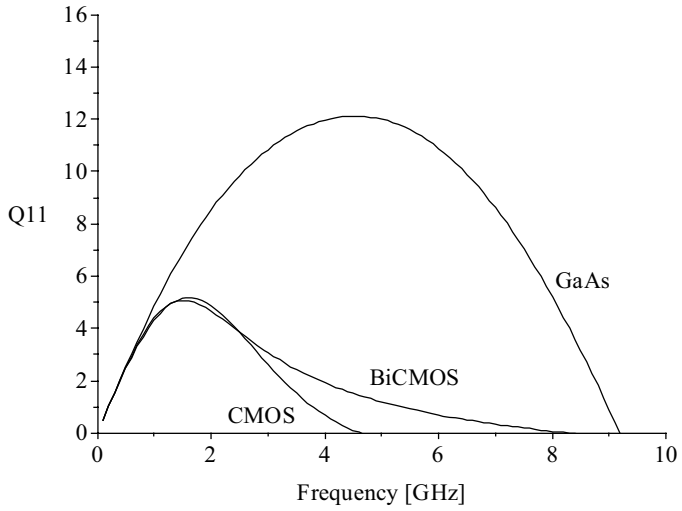

Figure 5.6. Impact of substrate material on inductor characteristics. The test device is a five-turn square device and the curves are achieved with an EM-simulator. Only the substrate properties are altered in each case. The Q_{11} curves depict self-resonance frequencies and clearly demonstrate the collapse in the CMOS case. The impact of a lossy substrate at high frequencies is distinctive.

5.2.3 Ground Shielding

Since capacitive losses in the substrate are a severe problem, a rather straightforward idea is to add a conductive shield beneath an inductor. Capacitive coupling to the substrate is now omitted. However, the parasitic capacitance to the shielding layer is large and the self-resonance frequency of the inductor collapses. Second, in a uniform ground shield eddy currents are free to flow, and the inductance value of the inductor is reduced as a result of mutual coupling to these eddy currents. In [5.36] it was suggested that the ground shield could be cut into slides to avoid eddy currents. Since then several papers have been published on this matter. A patterned ground shield can be implemented using a poly-silicon layer [5.36]-[5.41], lowermost metal [5.41]-[5.42], or n-well [5.43]-[5.44]. The shape of the ground shield has an impact on the performance, and a general rule is to avoid closed paths where eddy currents could flow [5.36],[5.37],[5.42]. In some cases it has been argued that ground shielding does not improve the inductor characteristics [5.43]. Indeed, if the distance from the inductor to the patterned ground shield is very small, the parasitic capacitance becomes very large and the self-resonance frequency decreases. As a result, at the frequency of interest the quality factor is not increased. Furthermore, despite patterning, small eddy currents flow in the shield segments, and in addition, the magnetic field is attenuated in the ground shield layer. These cause a reduction in the inductance value, as well as frequency dependency. Therefore, for attenuating these eddy currents a somewhat resistive shielding is better than a highly conductive type [5.41], and a thin layer is preferable [5.36]. Generally, it can be noticed that the best method for efficient ground shielding is technology-dependent. In modern multi-metal-layer processes a patterned ground shield is located rather far away from the metal layers. Thus, a reduction in the self-resonance frequency and in the inductance value is acceptable and ground shielding is commonly used. Figure 5.7 shows a comparison of various shielding options implemented using the *VTTB8* process. It is worth commenting that this process is an old-fashioned one, and

both the metal 1 and polysilicon layers have a relatively high sheet resistance. Thus, although here the shielding clearly makes things worse, one cannot draw conclusions for other processes. I have also ensured that the poor performance is not caused by improper layout design. That is, there are no paths for the eddy currents to flow.

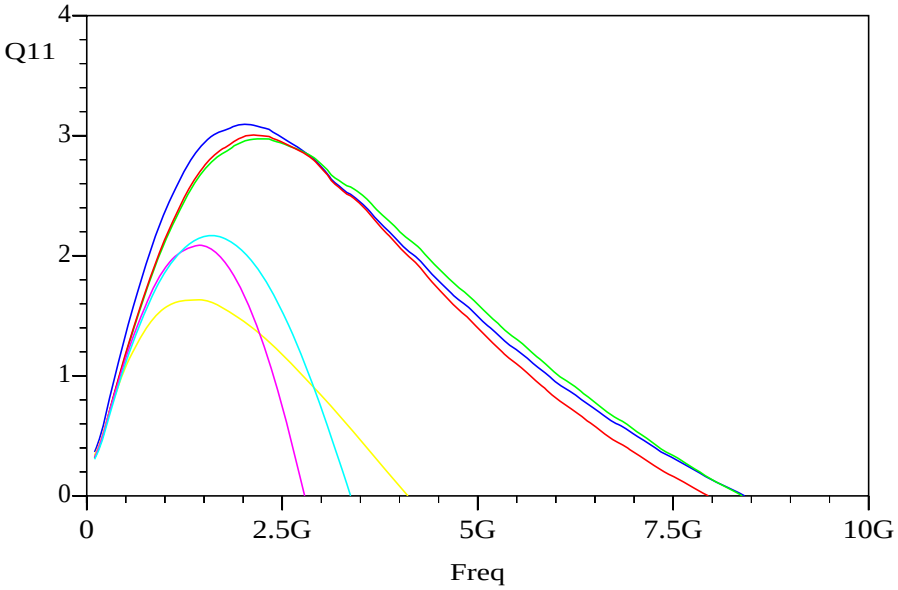

Figure 5.7. Comparison of some inductors fabricated in the *VTTB8* process. The test device is a five-turn metal-2 square inductor with W=15 μm and S=2μm. The green curve represents a pure metal-2 structure. The blue one has a continuous via for coupling both metal 1 and metal 2 together. The red one is a metal-2 inductor with an n-well beneath the inductor, yellow has a solid metal-1 ground shield, pink represents an inductor with a metal-1 patterned ground shield, and cyan has a polysilicon patterned ground shield. As it appears, in *VTTB8* a simple metal-2 inductor gives the best results.

5.2.4 Dummy Patterns

In modern processes, with as many as six to eight metal layers, the planarity of the metal surface is crucial. Good planarity is achieved by having a high metal density in all layers. It means that no large areas without metal filling are allowed. After the completion of the layout design, an automated tool is used to generate the so-called dummy metal patterns all over the die. Thus, a large number of small metal objects also appear into the vicinity of the inductors. These tiny metal pieces interact with the inductor. They provide a capacitive route to the substrate, thus increasing the parasitic capacitance of the inductor. Furthermore, small eddy currents flow in these objects as well and result in a slight reduction both in the inductance value and in the Q-value [5.45]- [5.49]. To reduce these effects, the dummy patterns should be as small as possible and placed as far away from the inductor as possible. In practice, these effects are quite weak and inductors in these modern processes show better performance than in the older technologies. Dummy patterns pose a design challenge, since they are not defined prior to the final layout and therefore it is not known exactly where they will appear. The best solution for a scrupulous designer is to draw the dummy patterns into an inductor cell manually and, if possible, model the device with these same patterns.

5.2.5 Symmetrical Layout

When a device is driven with a differential excitation, its effective parasitic capacitance and resistance are reduced, and as a result, both the self-resonance frequency and Q-value are

increased [5.50]-[5.52]. This can be understood by considering the equivalent circuit depicted in Figure 5.11. As explained in [5.51], in the case of differential excitation the substrate impedances appear in series, and thus the resistance values are doubled and capacitance values halved. In particular, if the structure of the device takes advantage of differential excitation by having a symmetrical layout, the increment in the Q-value is clear. Even in the case of a lossless substrate, a symmetrical device favors a slightly better internal mutual coupling, thus having a higher Q-value. Mutual coupling in a symmetrical device is discussed further in Section 5.3. Finally, a problem in differential circuits that have two single-ended inductors instead of one symmetrical one is that the mutual coupling between the two inductors is not properly modeled and this may have an impact on the circuit characteristics. If particularly careful work is done, one should carry out a post-layout EM-simulation to find out the amount of mutual coupling. By using a single symmetrical inductor this problem is avoided. Figure 5.8 shows differential and single-ended Q_{11} plots for a symmetrical inductor.

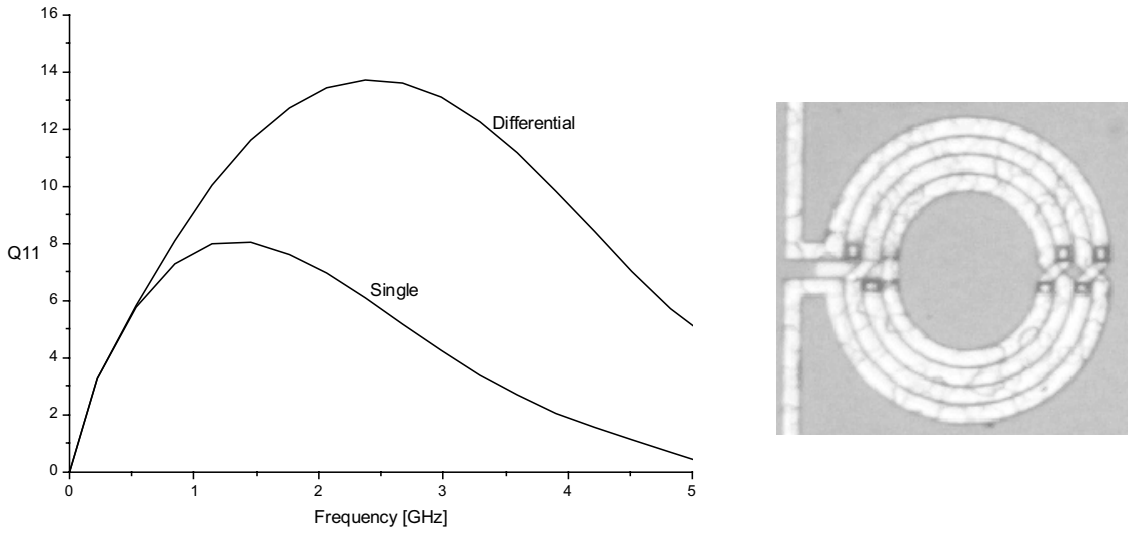

Figure 5.8. Measured differential and single-ended Q_{11}-plots for a symmetrical inductor. On the right, the layout of the inductor is depicted. The four-turn 6-nH inductor fabricated in *ATMEL's SiGe1* HBT process has W=22 μm and S=3 μm.

5.2.6 Stacked Inductors

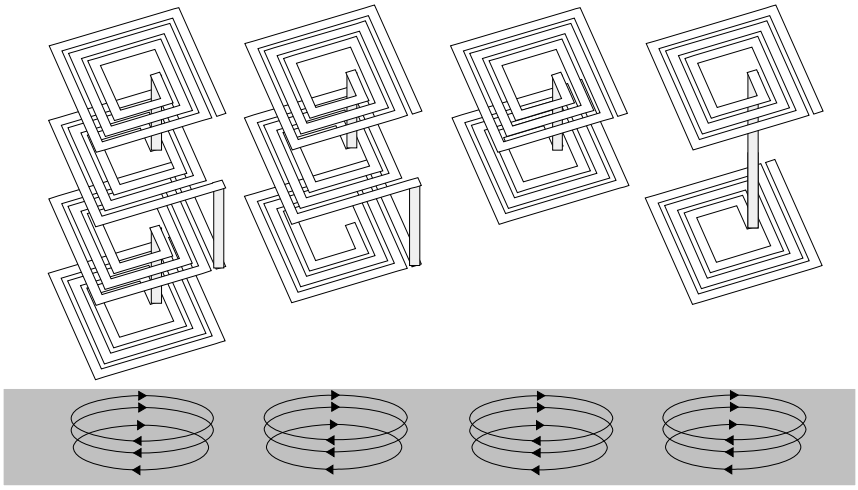

Figure 5.9. Some stacked inductor variants in a four-metal process. The eddy currents in the substrate are equal in each case.

Planar inductors occupy a substantially large die area, and if a particularly high inductance value is desired, the die area becomes a severe problem. Especially in compound technologies and in sub-200-nm silicon technologies, die area is extremely expensive. In multi-metal-layer processes it is possible to stack several spiral inductors on top of each other as depicted in Figure 5.9. A two-layer structure for MMIC use was first reported in [5.53] and a multi-layer case in [5.54]. Eventually, in GaAs technologies such a structure appeared as a standard component in a foundry library [5.2]. Recent studies on silicon are given e.g. in [5.32],[5.40],[5.55]-[5.58]. The main problem in stacked inductors is the capacitive coupling between the layers, and the resulting low self-resonance frequency. This issue was thoroughly studied in [5.55]-[5.56]. For a two-layer system the authors derived the following results:

$$L_{tot} = L_1 + L_2 + 2M \quad and \quad C_{eq} = \tfrac{1}{12}(4C_1 + C_2) \tag{5.18}$$

In the most simplified case L_1=L_2=L and the mutual coupling is assumed to be very strong, i.e. M≈L. Then, L_{tot}=4·L. C_1 is the capacitance between the inductor layers and C_2 is from the lower inductor to the ground. It can be concluded that by adding separation between the layers (reducing C_1) C_{eq} can be kept small, although C_2 is increased. In general, the precise study of multi-layer structures requires EM-simulations, and as the problem set-up is indeed manifold, it is a challenging field. Once again, it must be emphasized that the optimum structure is highly technology-dependent. In *VTTB8*, a five-turn inductor has a 4.2-nH inductance value and the same geometry as a stacked structure generates 11 nH. Three-turn cases generates 1.5 nH and 3.9 nH correspondingly. Unfortunately, metal 1 has such poor characteristics in this process that stacked inductors do not have an acceptable performance.

5.3 Equivalent Circuits and Parameter Extraction Procedure

Inductor characteristics as a set of two-port S-parameters are achieved either from the measurements or as a result of EM simulation. These parameters can be readily used for circuit simulation. However, it is more convenient and user-friendly to extract an equivalent circuit. As will become apparent, the equivalent circuit does not exactly represent the physical device, and hence, some loss of accuracy results. Therefore, various comparisons, such as Q-plots, should be derived directly from the two-port parameters. It is germane to emphasize that the equivalent circuit can only be as accurate as the source of the data. Therefore, EM simulations are discussed in detail in a later section. On-wafer measurement techniques are well established, so I will not discuss them in detail here. There are, however, several pitfalls regarding their practical aspects, so the utmost care is needed. Wartenberg's text [5.59]-[5.60] provides a good source for information on the measurement apparatus, calibration methods, and de-embedding techniques. In addition, the manufacturers of the measurement apparatus (e.g. *Cascade Microtech*, *PicoProbe*, *Agilent*) provide application notes and tutorial-level papers on these issues. A couple of practical comments are worth making here. First, remember to carry out the DC measurement in conjunction with the S-parameter measurement. An ohm-meter can be used as an indicator for a good probe tip contact and the result alleviates the extraction procedure. It also reveals when the aluminum oxide on top of the bonding pad is adequately broken. Second, calibration techniques have a limited bandwidth. For instance, the commonly used SOLT (short-open-load-thru) suffers from non-ideal standards at higher frequencies and TRL (thru-reflect-line) covers only three octaves as a result of its transmission line nature [5.59]. If broadband measurement result is desired, it should be performed at least in two steps. As an example, a typical layout for device parameter extraction is shown in Figure 5.10.

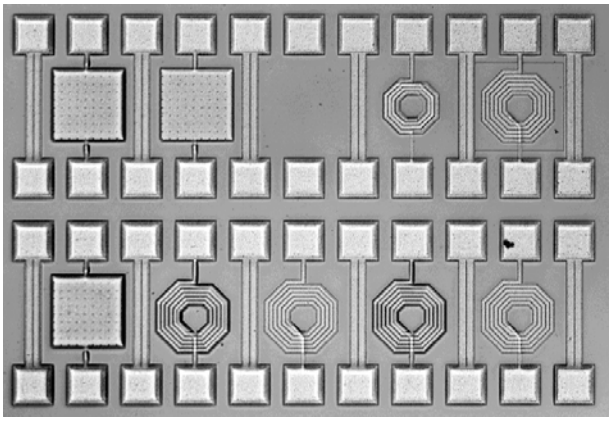

Figure 5.10. A typical test set-up for device parameter extraction. The empty slot is used for de-embedding the effect of the pads. The five inductors here differ in physical structure, while the geometry remains the same. The smaller sixth one is a stacked inductor. The three square structures are metal-insulator-metal capacitors.

Figure 5.11 depicts the most commonly used equivalent circuit topology and how the y-parameters are related to this π-network. Z_{sub} indicates the substrate impedance. The inductors are generally used at such a low frequency, compared to their size, that a lumped model is adequate, and a distributed model is not needed. More intricate models are occasionally used for representing frequency dependencies [5.61]-[5.65]. The most straightforward method to extract the equivalent circuit parameters is to use the optimization routines available in various circuit simulators. One might expect to get accurate results easily with this method. However, this is not the case. The problem is that the secondary parameters (C_f, C_{ox}, C_p, R_p) have a large deviation and consequently the optimization routine fails to get a good fitting. Second, as there is frequency dependency in L and particularly in R, it is hard to describe a correct optimization procedure. As a result, the inductance value remains uncertain. Minor changes in the optimization routine are reflected as fairly large shifts in the inductance value. This problem can be reduced with weighting factors in the optimization routines, and yet the results still remain uncertain. Because of this problem, more sophisticated techniques should be used for parameter extraction. Luckily, the π-network allows us to extract each section individually, thus reducing the number of independent parameters.

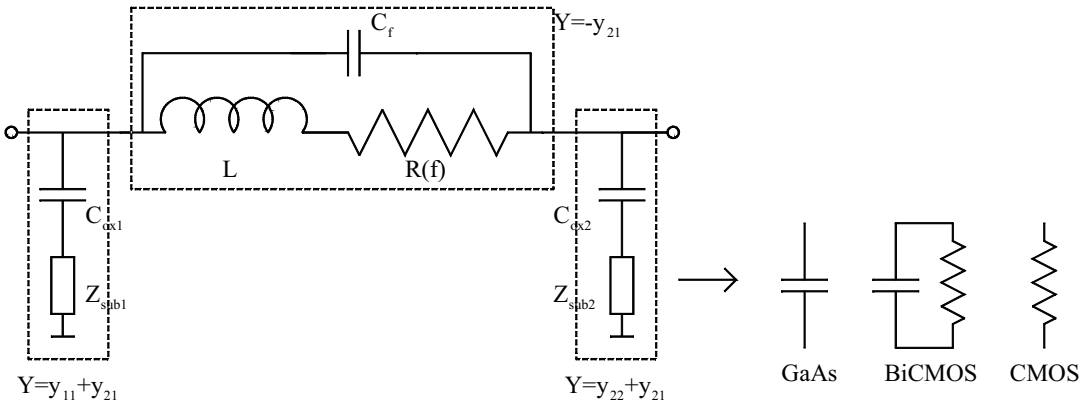

Figure 5.11. Equivalent circuit for a monolithic inductor and the substrate models.

The simplest case, which is actually rather commonly used, is to simply omit the fringing-field capacitance C_f and calculate the parameters L and R directly from y_{21}. Unless the parasitic capacitance C_f is insignificantly small, this simple method creates an incorrect non-physical frequency-dependent inductance caused by the L-C_f resonance. The effective losses also

increase more rapidly than the actual frequency-dependent series resistor, and this may give an incorrect impression of this matter. To put this in other words, the parameters L_{eff} and R_{eff} are simply used as an exact mathematical representation of y_{21}.

$$L_{eff}(\omega) = \mathrm{Im}\left(\frac{1}{-y_{21}}\right)/\omega \tag{5.19}$$

$$R_{eff}(\omega) = \mathrm{Re}\left(\frac{1}{-y_{21}}\right) \tag{5.20}$$

When the parasitic capacitance C_f is included, the extraction formulas are

$$L(\omega) = \mathrm{Im}\left(\frac{1}{-y_{21} - j\omega C_f}\right)/\omega \tag{5.21}$$

$$R_s(\omega) = \mathrm{Re}\left(\frac{1}{-y_{21} - j\omega C_f}\right) \tag{5.22}$$

Now, we have three unknowns but only two values at each frequency. Therefore, the direct calculation of these parameters is not possible. Actually, we have the pairs (L,C_f) and (R_s,C_f), which describe the original data accurately with *any arbitrary* value of C_f. This issue is illustrated in Figure 5.12, where the measured inductor characteristics are depicted for several chosen values of C_f. It is not possible to solve a system with two frequency dependent parameters without any additional information, and hence, we do not have any exact method to extract C_f. A common method is to assume L as frequency-independent and use L_{eff} extracted from the low-frequency result to calculate C_f. The self-resonance frequency ω_{SR} is found at L_{eff}=0, and C_f is given by

$$C_f = \frac{1}{L_{eff,LF} \cdot \omega_{SR}^2} \tag{5.23}$$

This is not a precise method since inductance is, at least to some extent, frequency-dependent and losses have a role in the exact definition of ω_{SR}. Furthermore, in many cases ω_{SR}, in the L_{eff}=0 sense, is far beyond the measurement band and this method is not applicable. Despite these limitations, the method often works in practice and gives a good fitting. Such a value for C_f is achieved that the inductance value actually decreases slightly with frequency, thus improving the broadband matching. The second method is to use Equation 5.21 for two adjacent frequency points at a time and assume a constant inductance value within these two points. The resulting third-order polynomial equation gives C_f:

$$P^3(C_f) = 0 \quad \Rightarrow \quad C_f = f(\omega_1, y_{21,\omega 1}, \omega_2, y_{21,\omega 2}) \tag{5.24}$$

This method suffers from numerical problems. By using a large number of data points and averaging, a reasonable estimation for C_f is achieved. The third method is to use an optimization routine for a constant L – constant C_f – $R_s(\omega)$ system. For the five-turn metal-2 inductor in the *VTTB8* process the first method gives a capacitance value of 62 fF, the second one gives 52 fF and the third one 57 fF. As Figure 5.12 depicts, a value around 50-60 fF corresponds to a slightly decreasing inductance value.

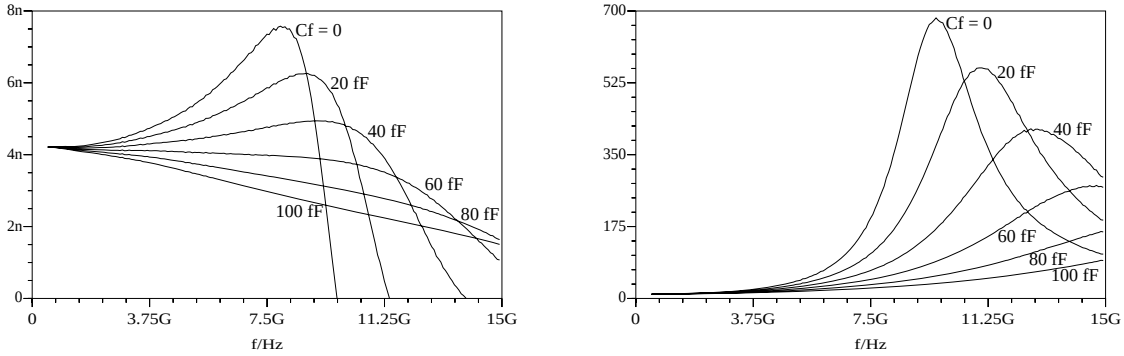

Figure 5.12. Extracted L (on the left) and R with several chosen values of C_f. The device is a five-turn metal-2 inductor from *VTTB8*.

The loss mechanisms discussed previously could be combined into a single series resistance:

$$R_s = R_{DC} + R_{skin}\sqrt{\frac{f}{f_{c1}}} + R_{crow}\left(\frac{f}{f_{c2}}\right)^2 + R_{eddy}\left(\frac{f}{f_{c3}}\right)^2 \tag{5.25}$$

where f_c stands for the corner frequency and is a scaling factor unique for each physical phenomenon. Although complete, this equation includes seven independent parameters and is therefore impractical for parameter extraction. In [5.9], a simplified version was proposed:

$$R_s = R_{DC}(1 + k_1 f^{k_2}) \tag{5.26}$$

Here, R_{DC} is a measurement result, or calculated from R_{eff} at low frequency, and only two fitting parameters are required. This curve has enough flexibility and gives good matching for $R_s(\omega)$ in a frequency range below the self-resonance. Frequency dependent elements in the equivalent circuit may cause some practical problems in simulations, such as poor convergence. Therefore, R_s is commonly approximated simply with a constant value at the frequency of interest. A small error in the DC analysis will generally have an insignificant impact. On the other hand, the losses at higher harmonics are underestimated. An alternative is to use a particular network to represent the frequency-dependent losses [5.61]-[5.65].

The capacitor C_{ox} related to the insulating layer beneath the inductor and the substrate network can be extracted using a similar procedure as for inductance. For a highly conductive CMOS case a resistor is a sufficient model for Z_{sub}. For the BiCMOS case a parallel R_p-C_p is used and for insulating substrates a capacitor is adequate [5.66]. In practice, a tiny series resistor improves the fitting in the insulating substrate cases, and thus both the low and the high end of the substrate resistivity scale are modeled with a series RC network. The extraction formulas are

$$C_{ox1}(\omega) = \left[-\omega \cdot \mathrm{Im}\left(\frac{1}{y_{11} + y_{21}}\right)\right]^{-1} \tag{5.27}$$

$$R_{p1}(\omega) = \mathrm{Re}\left(\frac{1}{y_{11} + y_{21}}\right) \tag{5.28}$$

In the BiCMOS case we have a three-parameter system: C_{ox} – C_p – $R_p(\omega)$. As previously, we may have only one frequency-dependent parameter for exact extraction, and it is R_p since it is

important to describe the frequency variation of the losses. Furthermore, it is a reasonably accurate assumption to consider capacitors as frequency-independent. Here, a fitting procedure is the most appropriate method. It appears that $R_p(\omega)$ is usually quite flat above 1 GHz, as shown in Figure 5.13, and can be approximated with a constant value. Once again, this simplifies the implementation of the equivalent circuit, although some loss of accuracy results.

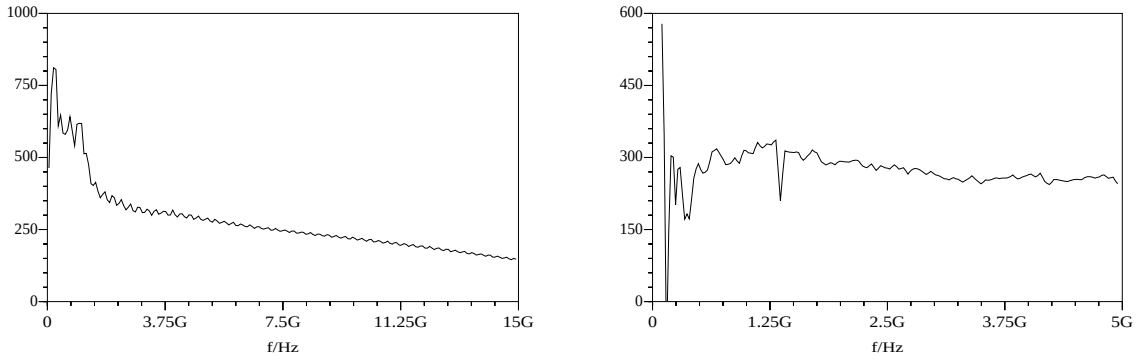

Figure 5.13. The extracted substrate resistance for the 4.2-nH *VTTB8* inductor is shown on the left, and on the right the same is shown for an 8-nH inductor fabricated in *ATMEL*'s *SiGe1* process.

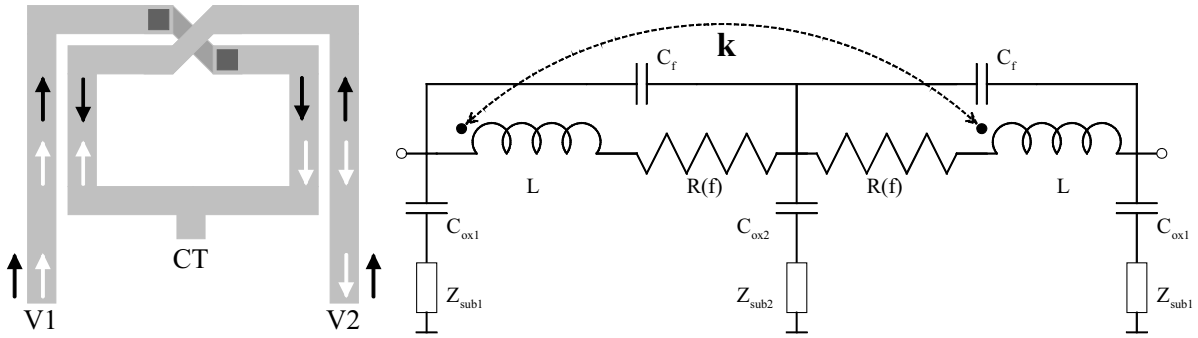

Figure 5.14. A symmetrical inductor and an equivalent circuit for it. The black arrows depict the flow of common-mode excited currents and the white ones are for differentially excited currents.

A conceptual symmetrical inductor structure is depicted in Figure 5.14. The inductor is excited with the signals V1 and V2, and the center tap "CT" is considered as a ground node. Usually, this node is either connected to the ground or supply rail. The input signals carry both differential and common-mode signals, i.e. $V1=v_{comm}+v_{diff}$ and $V2=v_{comm}-v_{diff}$. The black arrows illustrate the flow of the common-mode current and the red ones are for the differential current. In adjacent strips the common-mode current flows in opposite directions and therefore the inductance value is reduced. In contrast, the differential current flows in the same directions and the inductance value is increased. If a coupling coefficient k is defined, the inductance seen by the differential excitation is

$$L_{diff} = L(1+k) \tag{5.29}$$

and for the common mode case it is

$$L_{comm} = L(1-k) \tag{5.30}$$

The mutual inductance M is defined by $M = k \cdot L$ and $0 \leq k \leq 1$. Typically, the coupling coefficient k is in the range 0.3 – 0.8 depending on the device geometry and technology. A double-π circuit model for a symmetrical inductor is presented in Figure 5.14. Note that if the mutual inductance is excluded from the model, it is not able to describe the inductor impedance

for common-mode excitation correctly. One problem is that if the device characteristics are measured with an ordinary two-port measurement, it is not possible to distinguish L and M. A three-port measurement is needed, or an EM-simulator can be used.

It can be asked how large the error is if the common-mode impedance is modeled incorrectly. Obviously, this depends on the circuit under study. I have studied this question by sweeping the coupling factor k in the inductor model in the range {0…1} and by scaling the inductance value so that the differential inductance value remains constant. Six cases were studied:

1) BJT-oscillator with linear LC-resonator
2) BJT-VCO with pn-junction varactor (a smooth tuning curve)
3) BJT-VCO with abrupt MOS-varactor
4) NMOS-oscillator with linear LC-resonator
5) NMOS-VCO with pn-junction varactor (a smooth tuning curve)
6) NMOS-VCO with abrupt MOS-varactor

Various cases, such as low-Q vs. high-Q inductors and various amounts of parasitic capacitance, were studied, and they did not have any major impact. It turns out that the level of the second harmonic is affected by the mutual coupling. Balanced bipolar transistor oscillators are almost immune to this problem, whereas the CMOS circuits are more sensitive. Table 5.3 includes simulation results for the sixth case. It can be concluded that in the case of CMOS oscillators with MOS varactors it is mandatory to include the coupling factor k in the symmetrical inductor model.

Table 5.3. MOS-VCO characteristics in the presence of the mutual coupling factor k in the resonator inductor.

k	Freq [MHz]	Vosc [Vpp]	N/C@100kHz [dBc/Hz]	HD2 [dBc]
0	2861	2.304	-106	-14
0.2	2863	2.193	-108	-12
0.4	2870	1.886	-104	-8
0.6	2801	2.843	-97	-8
0.8	2847	2.869	-95	-21

5.4 Analytical, Semi-Empirical and Scalable Models

At the dawn of our art many attempts were made to calculate the inductance value using a single closed-form formula. Terman's book covers some of them [5.67] and since then, many others have been developed, e.g. [5.68]-[5.73]. A equation that is commonly referred to was developed by Wheeler [5.74] and its modernized version [5.21] for a square inductor is

$$L = \frac{NT^2 a^2}{11D_{out} - 14a} \cdot 47 \cdot 10^{-6} \tag{5.31}$$

Here D_{out} is the outer dimension of the inductor and the parameter a is the mean radius, defined as the distance from the center of the inductor to the middle of the windings. A comparison to measured inductance values for some inductors is shown in Table 5.4. As observed, Equation 5.31 gives quite a good estimation for the inductance value. An uncertainty of about 10% is an adequate starting point for test device implementation or for EM simulations.

Table 5.4. Measured vs. calculated inductance values for some devices.

Substrate	Inductor dim. NT, Din, W, S	Measured value [nH]	Eq. 5.31 [nH]	Error [%]
GaAs	4, 47, 5, 2	1.7 [1]	1.8	6
BiCMOS	5, 55, 15, 2	4.2	3.8	10
CMOS	7.5, 0, 15, 5	7.7	6.5	16

[1] Value taken from the foundry manual

Grover's work [5.75] was the basis for a classic paper by Greenhouse [5.76], where a fundamentally different approach was adopted. In the Greenhouse method the structure under study is divided into segments and each of them has its own self-inductance, as well as mutual coupling to all other segments. For a rectangular bar with dimensions *w, t,* and *l* the partial self-inductance can be approximated by:

$$L_s = 0.002 \cdot l \left[\ln\left(\frac{2l}{w+t} \right) + \tfrac{1}{2} \right] \tag{5.32}$$

The mutual coupling between two bars at a distance *d* can be approximated by

$$M = 0.002 \cdot l \cdot \left[\ln\left(\frac{l}{d} + \sqrt{1+\frac{l^2}{d^2}} \right) + \frac{l}{d} - \sqrt{1+\frac{l^2}{d^2}} \right] \tag{5.33}$$

The total inductance is $L_{TOT} = \sum L_s + \sum M_p + \sum M_n$ (5.34)

where M_p stands for all the combinations of positive mutual couplings and M_n is for the negative ones, correspondingly.

Particularly for a rectangular layout, the method results in an easy method for calculating the overall inductance. However, as the number of unit sections increase the calculation of the mutual couplings becomes tedious and therefore this method requires the use of a computer program.

The physical bases for parasitic elements are quite obvious and we have already discussed matters concerning resistive losses. The capacitance C_{ox} in the equivalent circuit can be estimated by calculating the wiring area (w·l). The capacitance C_f is related to the overlapping area of the upper and lower metal windings and to the vertical sidewall capacitances. These issues are covered in many papers, such as [5.21],[5.69],[5.72],[5.77]-[5.81].

The physical-based modeling that was very briefly discussed just previously gives a basis for establishing scalable inductor models. Instead of using the physical-based equations directly, they are usually expanded with a set of correction factors in the form of polynomial equations in order to improve the accuracy. Thus, the resulting inductor library may include as many as tens of parameters, and hence, may appear quite fuzzy.

As an example, I will here demonstrate the development of a scalable model by establishing a simple model for octagonal symmetrical inductors with the *MAS20B* process provided by *Micro Analog Systems*. *MAS20B* is an integrated passive device technology (IPD) where the passive devices are monolithically fabricated on top of a quartz substrate and the active devices, such as a CMOS chip, are added using either the flip-chip technique or wire bonding. Molybdenum, aluminum, and two layers of copper are fabricated on top of the quartz substrate. The process offers high-quality inductors, high-density capacitors, low-R_{sheet} molybdenum

resistors and high-R_{sheet} thin film resistors. An automated EM simulation environment was used in this development work and it will be discussed in detail later. It must be emphasized that the accuracy of the model is inevitably reduced when we shift from measured or simulated S-parameters to an LRCM model, and further into a scalable model. Therefore, in my modeling approach the end user has access to all these levels and is able to use different model approaches in different phases of circuit design. A set of 130 symmetrical octagonal inductors were simulated with the number of turns (NT) ranging from one to five and the metal width (W) ranging from minimum (15μm) to 30 μm in increment steps of 5 μm, and the inner dimension had a minimum of D_{in}=5W and increment step of 25 μm. The strip-to-strip spacing (S) was kept to a minimum. The devices were simulated as three-port devices and equivalent circuit parameters were extracted.

Figure 5.15 shows how the inductance value is related to the total length *l* of the inductor. This can be modeled using a quadratic relation

$$L=\alpha\cdot l+\beta\cdot l^2 \tag{5.35}$$

α and β are found for each case by curve fitting and can be related to the strip width using linear relations

$$\alpha=c_1(NT)-c_2(NT)\cdot W \tag{5.36}$$
$$\beta=c_3(NT)+c_4(NT)\cdot W \tag{5.37}$$

Here the inductance value is calculated using the length, width, and four coefficients. This results in an inaccuracy of 5% or less. In typical foundry models more correction factors are used and the accuracy is therefore better.

The coupling factor k for cases NT=2…5 is shown in Figure 5.15. Here a simple first-order fitting equation is adequate:

$$k=c_5(NT)+c_6(NT)\cdot l \tag{5.38}$$

Actually, the variation in the k-factor is quite small and even a fixed value k=0.4 would result in an adequate model.

The capacitance Cf (Fig. 5.16) is given with an inaccuracy of about 10% by $Cf=c_7\cdot l$. (5.39)

Note that in the *MAS20B* process the dominant parasitic capacitance is the vertical sidewall capacitance, in contrast to ordinary IC cases where the lateral capacitances dominate.

The frequency dependency of the series resistor can be implemented simply by letting the end user define the frequency of interest, and using fitting equations, similar to the ones used in the previous cases. Here I have taken a short cut and modeled losses only at 4 GHz. A small error is then introduced into the DC resistance but it has no impact in ordinary circuits. The series resistance is depicted in Fig. 5.16, and is calculated with

$$R_{@4GHz}=c_8(NT)+c_9(NT)\cdot l \tag{5.40}$$

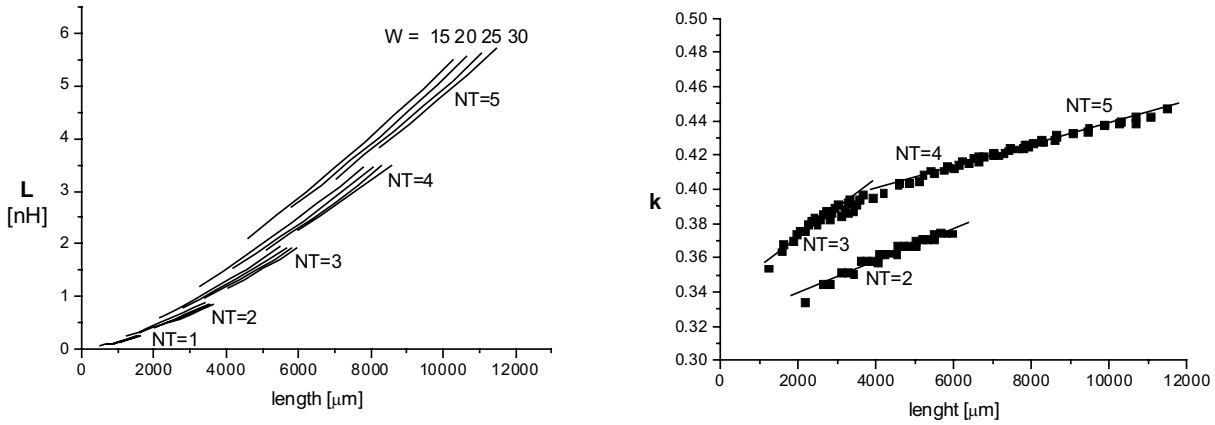

Figure 5.15. Left: Inductance value vs. total length for a set of symmetrical octagonal inductors. Right: Coupling factor k vs. total inductor length.

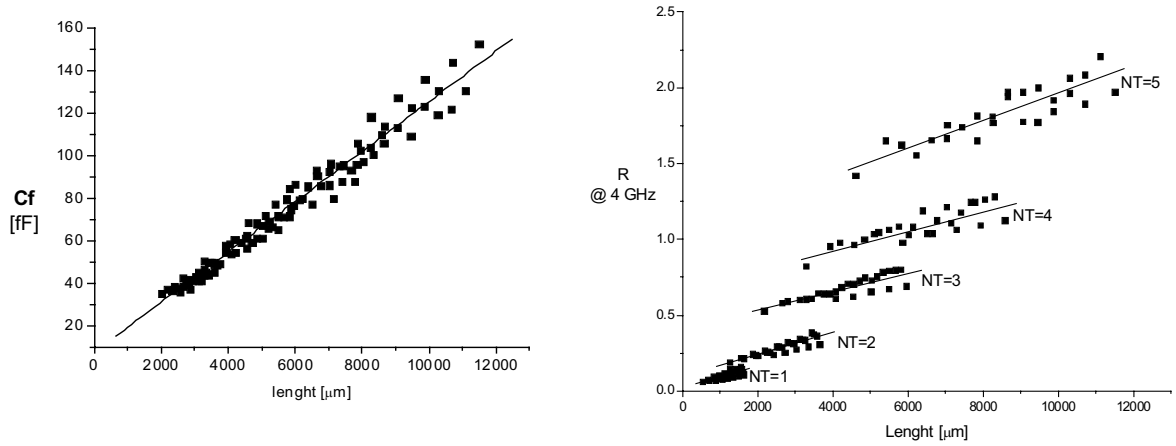

Figure 5.16. Left: Fringing-field capacitance Cf vs. total inductor length. Right: Series resistance at 4 GHz vs. total inductor length.

5.5 Electro-Magnetic Field Simulations

The electro-magnetic (EM) simulation techniques are essential since test die processing and measurements are tedious, time-consuming, and expensive. Furthermore, we can optimize the structure of the inductor with an EM-simulator or use it to predict the performance of an inductor in an arbitrary process. However, one should not take it for granted that the EM-simulation results are always correct. All simulators have certain limitations, flaws, and weird features. Equally, process parameters, and hence the technology description in an EM simulator, may differ from the correct values. Therefore experimental parameter extraction is required to check that the simulated and measured characteristics match. Second, the end user should study the properties of the selected simulator thoroughly and perform various comparative test simulations. Swansson's book [5.31] includes a description of various simulation techniques and their limitations. Niknejad [5.82] gives a detailed explanation of a freeware inductor simulation software called *ASITIC* and its limitations. In my own experimentally-oriented work I have used a commercial software *Momentum* from *Agilent Technologies*, and this section is solely based on it.

5.5.1 Methods of Momentum

Momentum is a so-called 2.5D simulator based on methods of momentum [5.83]. The physical structure of the device-under-study is described by a two-dimensional layout similar to an IC layout and by a technology description. The technology description is a pile of layers as depicted in Figure 5.17. Each metal layer is flat and is attached to a dielectric layer. Special vias are defined for supporting vertical currents. This simplification results in faster simulations with a lower memory requirement compared to truly 3-dimensional approaches. Second, the definition of device structure is easy. In this method the structure is meshed into unit cells (rectangles, triangles or polygons). Each cell has self-inductance, capacitance and loss, as well as electrical and magnetic coupling to all the other cells in the structure. The simulator then solves currents and voltages throughout the structure, and finally derives S-parameters for the excitation ports. In the basic simulation metals have zero thickness, and if the width-to-thickness ratio of the metal is small, the results are less accurate. To avoid this, a well-known trick [5.31],[5.84] is to represent a physical layer with two simulation layers and a combining via layer as depicted in Figure 5.17 for the topmost layer. In version 2003C of *Agilent ADS Momentum* this thick metal approach was automated and the mathematical accuracy was also improved [5.85],[5.86].

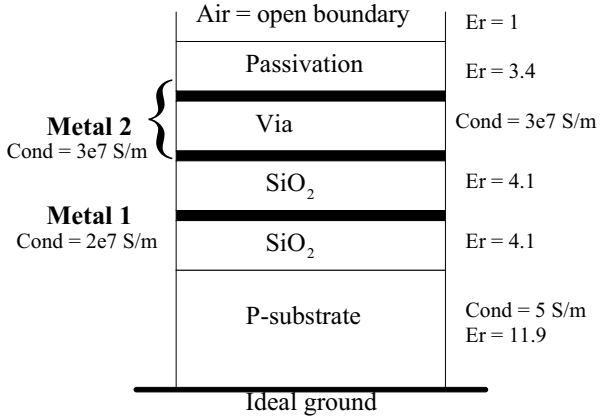

Figure 5.17. Technology description for a two-metal process. The topmost metal is considered thick and represented by two metal layers and a continuous via layer.

5.5.2 EM Simulations vs. Measurements

In general, the present view is that methods-of-momentum-based simulators are able to simulate the performance of a monolithic inductor with decent accuracy, assuming that the end user avoids possible pitfalls. However, to ensure that the simulator is used correctly and the process parameters are correct, simulation results must be checked with measured characteristics. I have compared the simulated and measured characteristics of a large variety of devices from several processes and found that the results agree well. For the sake of brevity, only some examples are given here. The comparison is performed here using the floating one-port parameters L_{eff} and R_{eff} (Eqs. 5.19 and 5.20). Furthermore, one should observe other parameters, such as substrate capacitance and loss, for best fitting. Those figures are omitted here for the sake of brevity.

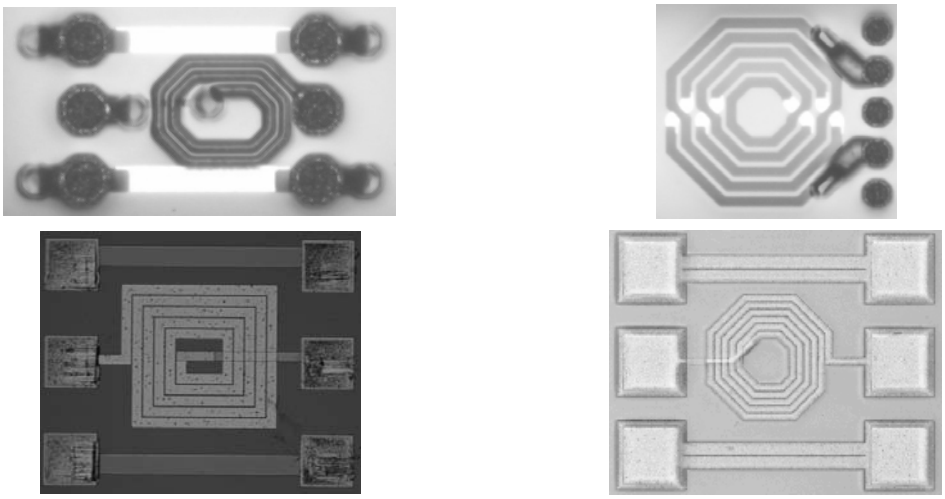

Figure 5.18. Microphotographs of some test inductors. In the upper row inductors on a quartz substrate are depicted. Test inductor A is shown on the left and inductor B on the right. In the lower row an inductor on a BiCMOS process (*VTTB8*) is shown on the left and a CMOS inductor is shown on the right. The pictures are not to the same scale.

A quartz substrate is used here as an example of an insulating substrate case. A set of eight inductors was fabricated in the *MAS20B* technology and two of them are depicted in Figure 5.18. EM simulation results are compared with the measurements in Figures 5.19 and 5.20. Very good agreement can be noticed. Particularly in the latter device, the low self-resonance frequency, caused by large lateral capacitance, is modeled accurately, thus indicating that lateral electrical (capacitive) coupling also takes place correctly in the simulations. Here both copper layers have been modeled as thick metals. *VTTB8* is used as an example of a BiCMOS process. A five-turn test inductor is shown in Figure 5.18 and the results are shown in Figure 5.21. Here the metals are modeled without thick metal extension. *MIETEC*'s *C05M* is a 0.5-µm CMOS process with three metal layers, a highly conductive substrate with a resistivity of 15 mΩ·cm, and a 4-µm thick epi-layer with a resistivity of 10 Ω·cm. A five-turn test inductor is shown in Figure 5.18 and its characteristics are shown in Figure 5.22. Here too the metals are modeled without thick metal extension. In the case of highly conductive substrate it is more challenging to achieve a good fitting. The situation is improved if a fictitious metal layer is attached onto the substrate and has a conductivity equal to that of the substrate. Luckily, the trend in new advanced CMOS technology generations is to use high-resistivity substrates. Thus, the problems related to highly conductive substrates are becoming obsolete.

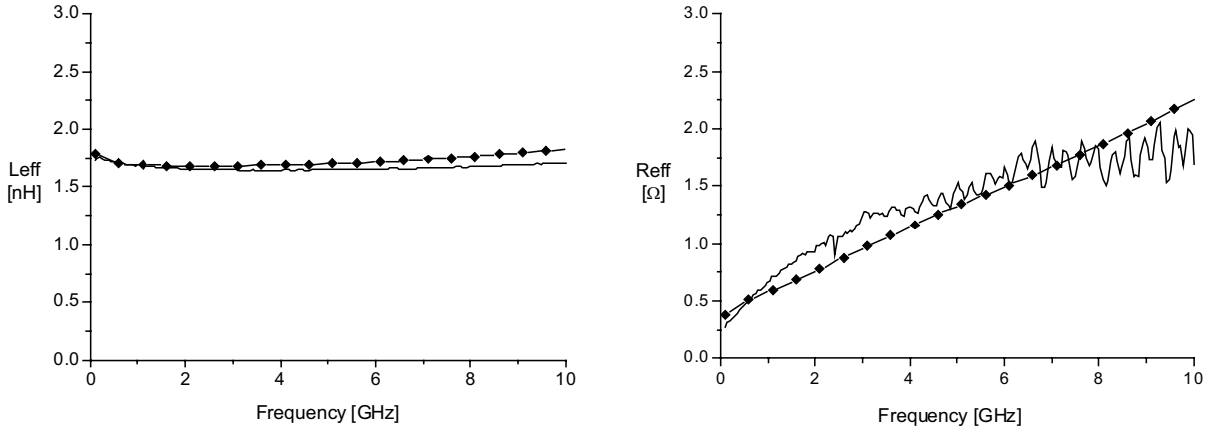

Figure 5.19. L_{eff} and R_{eff} for the test inductor A on a quartz substrate. The plain curve represents the measured results and the simulated characteristics are labeled with a marker.

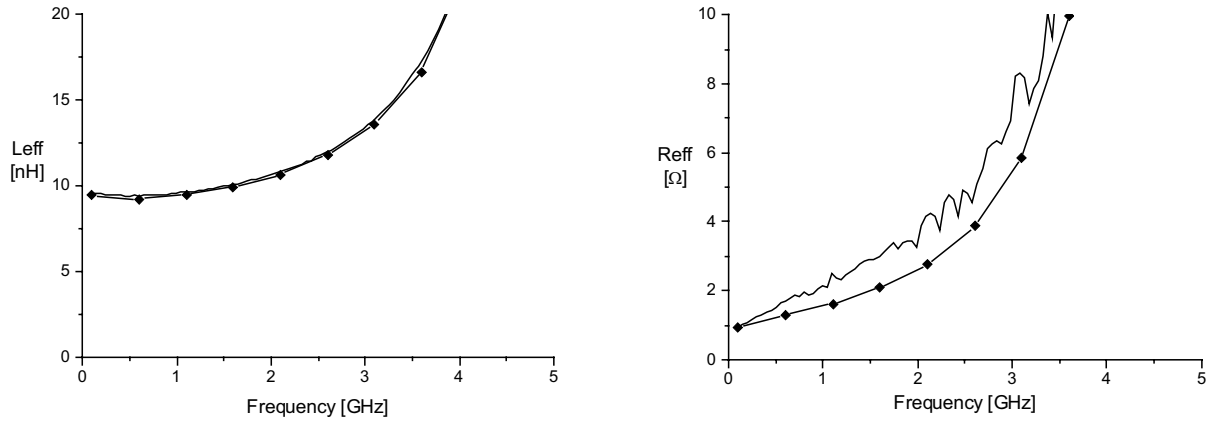

Figure 5.20. L_{eff} and R_{eff} for the test inductor B on a quartz substrate. The plain curve represents the measured results and the simulated characteristics are labeled with a marker.

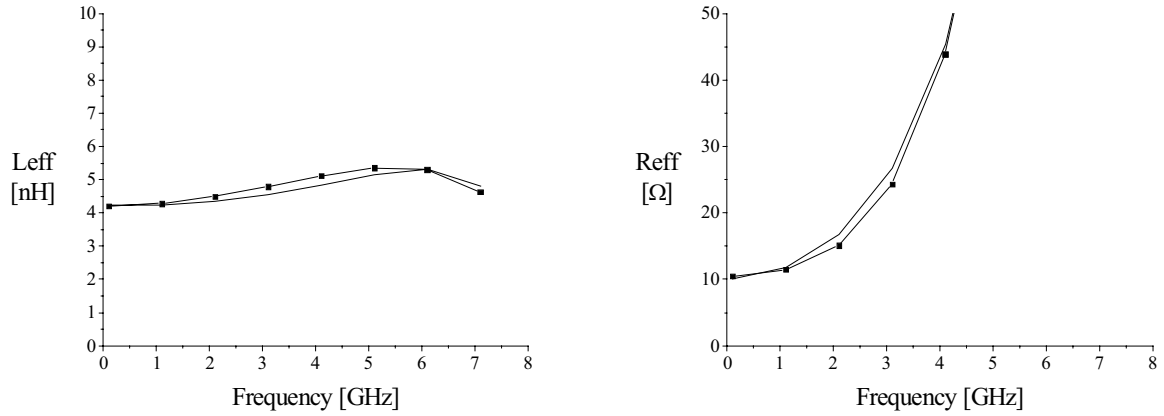

Figure 5.21. L_{eff} and R_{eff} for an inductor on a BiCMOS substrate. The plain curve represents the measured results and the simulated characteristics are labeled with a marker.

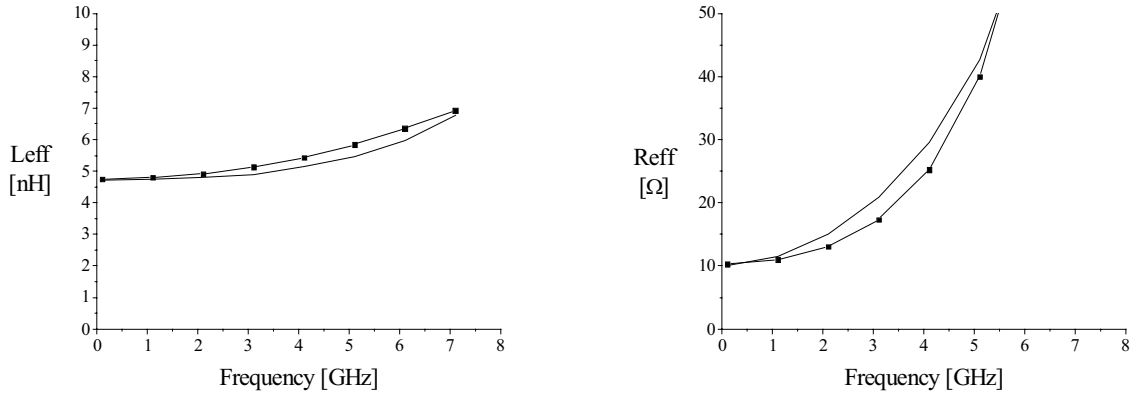

Figure 5.22. L_{eff} and R_{eff} for the *MIETEC* inductor on a highly conductive CMOS substrate. The plain curve represents the measured results and the simulated characteristics are labeled with a marker.

5.5.3 Automated Simulation and Parameter Extraction Procedure

Operating an EM-simulator manually is adequate for a small set of inductors. However, if devices with various sizes are to be compared, it appears that redrawing the inductor layout with slightly varied dimensions is particularly tedious. Furthermore, since each simulation takes from some minutes up to hours, interactive use is not possible. An automated simulation procedure is required to circumvent these problems. We have developed an automated EM-simulation tool using the Application Extension Language *AEL* of *Agilent ADS & Momentum*. The work was published in [5.87]. The structure of the software is depicted in Figure 5.23. The end user generates an input text file where each inductor is described with the number of turns (NT), inner dimension (Di), width of strip (W), spacing between strips (S), and the increment of strip width in each turn (inc). The last parameter enables the tapered devices to be studied. Then the geometry module uses these values to draw the device layout and finally the EM simulation is activated. The program runs as long as there are new lines in the input file. Each simulation result is stored into a unique S-parameter file named according to the input parameters. After all the simulations are done, end user interaction is required to start an *Aplac*-run. *Aplac* reads each EM simulation result, one file at a time, and extracts the user-defined parameters or characteristics, repeating this for all cases. The final result of this procedure is a component library where we have models for the inductors, as well as the original S-parameter files. EM-simulations do indeed take a considerable amount of time but it is essential that no human interaction is required. Post-processing using *Aplac* is a quick task. New processes are easy to study, simply by altering the technology description. New device geometries require some programming. At the moment we have geometry modules for single-ended square, octagonal and circular cases, and for the symmetrical square and octagonal devices with an ordinary layout and inverse layout proposed in [5.28].

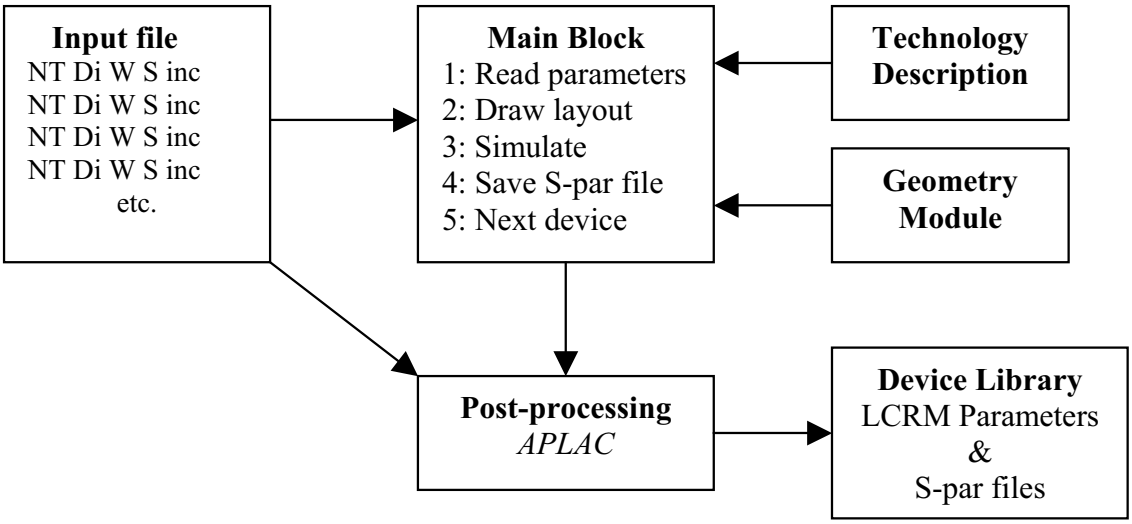

Figure 5.23. Flow diagram for an automated inductor simulation procedure.

5.6 Bonding Wires

Integrated circuits are commonly attached to the package or mounted directly onto the PCB with bonding wires. Often the bonding wires are considered as a problematic source of unwanted couplings, but they can be of use too. In VCO design they can be used as a resonating inductor. They offer a high quality factor and low parasitic capacitance. The main problems are reliability issues, cost, and manufacturing spread. Typically, bonding wires are made of gold or aluminum and have a thickness of 25 μm. A typical pad interval on an IC die

is about 100 μm and a commonly used small-scale-outline package (SOIC) has lead spacing of 0.5 mm. Figure 5.24 shows a microphotograph of a real case and Figure 5.25 describes four basic structures for bonding wires. The use of a long over-die bonding wire, proposed in [5.88], has faced doubts in industry and has not been generally accepted. Instead, Case B depicted in Figure 5.25, is compatible with the standard bonding process and can be used for establishing a balanced inductor for a differential VCO. Figure 5.26 illustrates a typical shape for a bonding wire [5.89] and shows how to approximate it with a linear three-segment model.

Figure 5.24. Microphotograph of bonding wires used to attach an IC to a package. In the middle, a balanced inductor for a VCO is established by bonding from two separate pads into the same package pin.

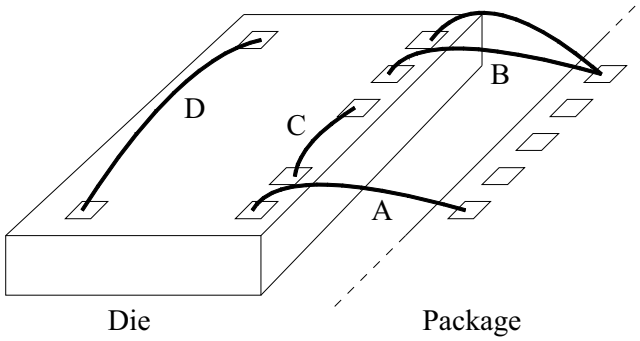

Figure 5.25.
Four basic bonding wire structures:
A) Conventional bonding wire
B) Bonding two IC pads to one package pin
C) Short pad-to-pad wire
D) Over-die pad-to-pad bonding

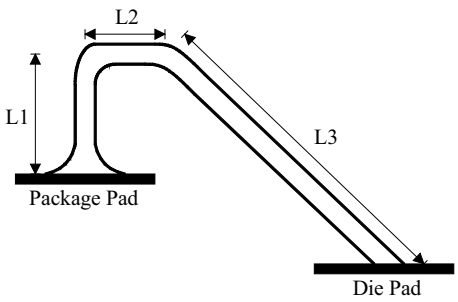

Figure 5.26. Standard model for a bonding wire.

A crude estimation of bonding wire inductance is simply 1 nH/mm. More precisely, the self-inductance of a straight long wire far away from the ground plane can be calculated with [5.75]

$$L = \frac{l}{5}\left[\ln\left(\frac{2l}{r}\right) - 0.75\right] \tag{5.41}$$

and the mutual inductance for two parallel wires is

$$M = \frac{l}{5}\left[\ln\left(\frac{l}{d} + \sqrt{1 + \frac{l^2}{d^2}} \right) - \sqrt{1 + \frac{d^2}{l^2}} + \frac{d}{l} \right] \tag{5.42}$$

Here l is the length of the wire, r is the wire radius, and d is the distance between two parallel wires. If l is given in millimeters, then L and M are in nanoHenries. As an example, two adjacent 1-mm wires with a 200-μm spacing have L=0.9 nH and M=0.3 nH. Hence, mutual coupling is of significance and must not be neglected. These formulas can also be applied to each section of the standard wire model in Figure 5.26 or for a set of wires, thus resulting in a Greenhouse-type analytical model for a bonding wire array [5.90].

Actually, the bonding wire inductance is smaller than predicted by the previous equations for the following reasons. First, a ground plane may exist beneath the bond wire, causing a decrease in the effective value of the inductance. Image current located at the opposite side of the ground plane causes negative mutual inductance [5.91]. Second, a curved wire has smaller inductance as a result of the mutual inductance cancellation of the different segments of the wire. The higher the arc of the wire is compared to the lateral length, the stronger this effect is.

In the balanced bonding wire inductor structure shown in Figure 5.24 the wires are not parallel at a constant distance. Instead, the wires close in and finally touch each other. By approximating such a structure with a triangular shape, and letting the angle between the wires be α, l being the wire length and d being the distance between the two non-common end points, the mutual coupling is expressed as [5.75]

$$M = \frac{l}{5} \cdot \cos\alpha \cdot \ln\left(\frac{2l + d}{d} \right) \tag{5.43}$$

As shown in Table 5.1 the skin depth at 2 GHz is only about 2 μm. Thus, ohmic losses related to a bonding wire are mainly caused by the skin effect, while the DC resistance is very small. Series resistance can be calculated with Equation 5.15. An aluminum wire has a series resistance of about 0.2 Ω/mm and the quality factor is about 50 at 2 GHz.

The previously expressed formulas are semi-empirical and are based on simplified geometries. In addition, high-frequency phenomena, such as the skin effect, proximity effects, and radiation, are not completely taken into account. If particular accuracy is needed, and reliable information on the exact dimensions of the bonding wire and its surroundings is available, then full 3-D EM-simulations are a recommended method for achieving an improved model [5.31],[5.92].

In [5.88] Craninckx estimates a process spread for a long bonding wire based on estimated deviations from the assumed shape of the wire and ends up with a 6% spread estimation for the inductance value. Lee has observed a spread of about 5% [5.93], whereas Svelto estimates a large spread of ±20% [5.94]. Another viewpoint is based on the comments of manufacturing experts: a bonding machine is able to feed the wire within an accuracy of 0.1 mm [source: private discussions]. Thus, for long wires deviation in the exact shape causes spread, and for short wires the variation in the exact wire length causes spread. This is in contrast to monolithic inductors where the process spread is so small that it can usually be neglected. In addition, in prototype development the height of the bonding wire arc is unknown and even the placement of the IC die inside the package cavity is uncertain. Thus, the value of the bonding wire inductor may differ from the expected one. These manufacturing-related issues can mostly be

solved in an industrial environment, but some amount of process spread will remain: according to [5.21], only about 1%. In my own experiments bonding wire-based VCOs had a 5% spread in the center frequency and VCOs with a monolithic inductor had only a 1% spread. All the dies in this work were from the same wafer.

Part and parcel of the bonding wire is a bonding pad and its structure and modeling. In a conventional pad in silicon technologies an electrical field penetrates into the lossy substrate beneath the bonding pad resulting in a lossy capacitor, and thereafter degradation of the bonding wire quality factor. Therefore, in modern processes the lowermost metal or poly-silicon layer can be used as a grounded shield. Thus, a model for such a bonding pad is a high-Q capacitor. Typically, such a capacitor is in the range 50-200 fF, depending greatly on the technology.

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6 Monolithic Capacitors

In the vast majority of LC-VCOs frequency tuning is accomplished with a variable capacitor (varactor, variable reactor), and hence this chapter also mainly focuses on those. A historical review of varactors is given in [6.1]. In silicon technologies the varactor can be of the pn-junction type or a MOS-structure, in the GaAs MESFET and HEMT technologies a metal-semiconductor Schottky diode is used, and in the GaAs HBT technology a pn-junction can be used [6.2]. In addition, frequency tuning, and particularly coarse tuning, can be done with the aid of a switched capacitor array. These are studied at the end of this chapter. Prior to the considerations of the details of varactors, some general issues are presented, and Section 6.1 deals with linear capacitors.

Figure 6.1 presents a simple model of a capacitor. It can be used both for linear and non-linear capacitors. Often device structures are such that the direct parasitic capacitance from node 1 to ground is so small that it can be neglected. Furthermore, in a detailed model series inductance Ls will be included. Three figures of merit can be defined for a capacitor:

$$Q_{cap} = \frac{1}{\omega C R_s}, \qquad Cap-ratio = \frac{C}{C_p}, \text{ and} \qquad Cap-density = \frac{C}{Area}.$$

Often capacitors and, particularly, varactors are used in such a fashion that node 2 is grounded. Then, the cap-ratio is an obsolete measure. On the other hand, if a floating capacitor is required then the cap-ratio is of particular importance and it may even turn out that the applied process does not offer capacitors with an adequate cap-ratio.

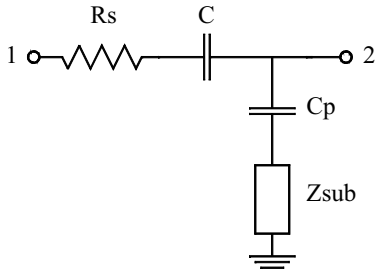

Figure 6.1. A simple equivalent model of a capacitor. The substrate impedance Zsub is the same as in Figure 5.11.

6.1 Linear Capacitors

Linear capacitors in IC technologies can be over-lay-type capacitors with a vertical electrical field or interdigitated structures with a lateral electrical field. The most common ones are ordinary plate capacitors. These can be formed between any two conductive layers isolated by an insulating layer. In double-poly processes a polysilicon-oxide-polysilicon capacitor offers the highest capacitance density. Because of the relatively high losses of polysilicon, metal-insulator-metal capacitors are favored in RF applications. In some advanced processes a special process step is provided for reducing the thickness of the insulating layer, thus increasing the capacitance density and C/C_p-ratio. Another method for increasing the capacitance density and C/C_p-ratio is to use multilayer "sandwich" structures, illustrated in Figure 6.2a. For instance, in a five-metal process metals 1, 3, and 5 would be connected together while metals 2 and 4 are then attached to the other terminal. The capacitance value of the plate capacitor is calculated with

$$C = \frac{Area}{thickness}\varepsilon_0\varepsilon_r + perimeter \cdot C_{ff} \tag{6.1}$$

Here C_{ff} stands for fringing-field ("side-wall") capacitance. It is related to the device geometry, area-to-thickness ratio, and the distance to the surrounding elements, and thus any exact measure is difficult to give. If the device geometry is the same as used in a test device, then C_{ff} can be embedded into the area capacitance. In other words, square capacitors, for instance, can be scaled to any reasonable dimension as long as the shape is not altered. If a foundry manual provides just a single value for the capacitance density, it is usually achieved by measuring a plate capacitor, and thus includes the fringing-field effect. An experimentally derived expression is often used in design kits for geometry variation, and in such cases it is imperative to find out the boundaries of this estimation. For instance, in one model the accuracy was good up to a width-length ratio of 3:1. Finally, it is always germane to keep in mind the process spread associated with plate capacitors. The thickness of the insulating layer varies both within a single wafer as well as from run to run, resulting in a process spread in the range of 5-50 %, while a typical value is 20 %.

Interdigitated or lateral flux capacitors, shown in Figure 6.2b, take advantage of the sidewall capacitance of adjacent metal strips. They have been used in the GaAs technology for a long time to fabricate accurate small-value capacitors [6.3]. In old-fashioned silicon technologies such structures were impractical since the parasitic capacitance was so large. Recently, it has been observed that in the very latest multi-metal-layer processes the lateral spaces between the metal lines in the same layer are smaller than the vertical spaces between the metal layers. Furthermore, the lateral dimensions are well controlled, thus providing small process spread, though the thickness of the metal and insulating layers does vary, and hence, these capacitors also suffer from process spread. Typically, the process spread is 10 – 20 %. By combining as many as six to eight layers it is possible to achieve a high-Q capacitor with a low parasitic capacitance and well-controlled value. In below-100-nm CMOS processes it often appears that these lateral-flux capacitors offer a higher capacitance density than the plate capacitors.

Both lateral and vertical field capacitors can be combined in various fashions. In [6.4] some combinations are depicted. The woven capacitor, shown in Figure 6.2c is an example of such a combination. It offers lower series inductance and a higher Q-value compared to the interdigitated structure, but the capacitance density is lower. Fractal capacitors [6.5] are a special case where the lateral field is maximized by trying to achieve an infinite perimeter offered theoretically by the fractal geometries. Though these do offer some increment in the capacitance density, they have not become popular, since they are difficult to model. In a general-purpose RF IC design kit device models and cell layouts should be easy to use, scale, and model. Therefore, clear standard structures are favored.

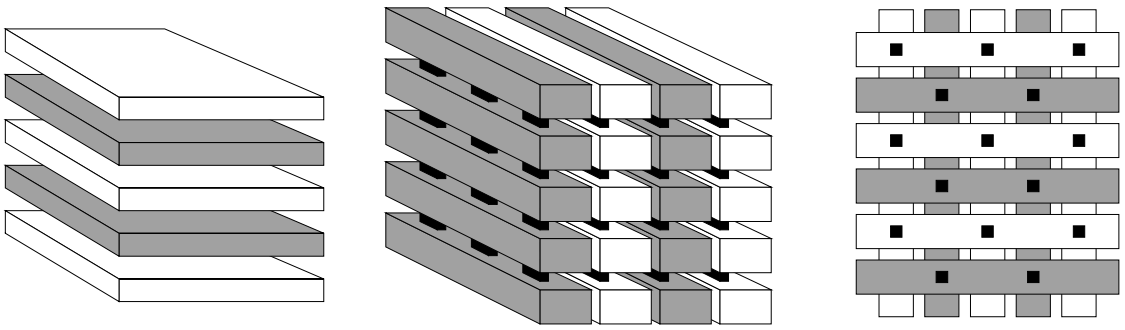

Figure 6.2. (a) Multi-layer vertical-flux plate capacitor. (b) Multi-metal-layer interdigitated lateral-flux capacitor used in advanced CMOS technologies. (c) Woven capacitor combines lateral and vertical capacitances.

Table 6.1 includes a selection of measurement results of test devices fabricated in some IC processes, as well as devices from foundry-provided design kits. Actually, several slightly different versions of the measured devices were implemented, but here only one typical case of each type is given for reasons of brevity and clarity. Furthermore, the quality factors of these devices are quite high, usually exceeding one hundred at 2 GHz. This means that the series resistance is very small, and thus sensitive to measurement errors. Particularly in silicon technologies aluminum pads are covered with native oxide, and this results in an unpredictable additional series resistance. With RF design below 5 GHz we can usually assume that the capacitors are simply high-Q devices, but at higher frequencies this rule is not valid anymore. Then one should pay attention to modeling issues, since in some cases the models in the design kits do not model the losses accurately. Furthermore, the interconnections to/from the capacitor may be a source of significant losses.

Table 6.1. Capacitor properties in some IC technologies.

Technology	Device	M/DK[1]	C/area [aF/μm^2]	C/Cp
2-metal 0.5-μm GaAs MESFET	Metal2 – metal1 plate capacitor	DK	520	210
2-metal 0.7-μm GaAs MESFET	Metal2 – metal1 plate capacitor	DK	400	120
2-metal 0.8-μm BiCMOS	Metal2 – metal1 plate capacitor	M	80	3
3-metal 0.5-μm CMOS	Metal 3&1 – metal2 plate capacitor	M	70	9
5-metal 0.35-μm CMOS	M5 & M3 – M4 & M2 Plate capacitor	M	150	8
3-metal 0.9-μm SiGe Bipolar	Metal 1 – salicided polysilicon plate cap [2]	DK	1100	37
4-metal 0.35-μm SiGe BiCMOS	Thin oxide MIM plate capacitor	DK	1000	31
6-metal 0.13-μm CMOS	Thin oxide MIM plate capacitor	DK	2400	200
6-metal 65-nm CMOS	M1-M5 interdigitated[3]	DK	910	15

1) M=own measurement, DK=design kit values
2) Here the Q-value at 2 GHz is only 25.
3) Cp is summed from both nodes in interdigitated capacitors

6.2 Schottky Varactor

The metal-semiconductor interface, depicted in Figure 6.3, forms a Schottky barrier junction diode. Such a diode is used in the GaAs technologies as a variable capacitor. Generally, the layout is derived from that of an interdigitated MESFET by connecting the drain and source terminals. The basic model of the junction capacitance is given by [6.6]

$$C(V) = \frac{C_0}{(1 - V/V_{BI})^{\gamma}} \tag{6.2}$$

Here C_0 is the capacitance at zero bias, V_{BI} is the built-in potential (~0.8V), and γ is a doping profile-related factor (~0.4 - 0.5).

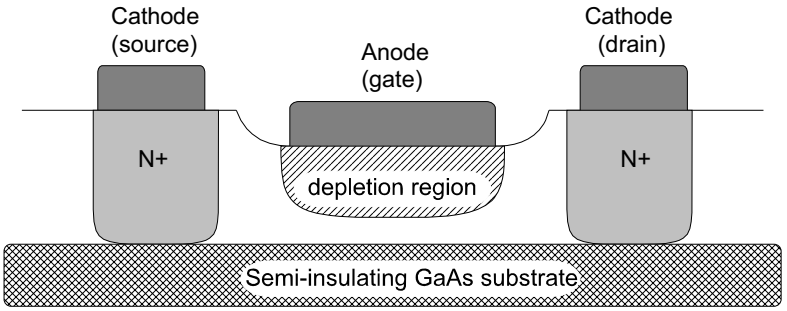

Figure 6.3. Cross-section of a Schottky varactor.

In many respects, such as in layout optimization and in modeling issues, the Schottky varactor resembles either a pn-junction varactor or MOS varactor, and since these will be discussed in detail, here only a brief introduction is given in order to avoid duplication. A particular issue here is the device performance when the channel region becomes depleted all the way thorough the channel region to the semi-insulating substrate. Then, the capacitance reduces to parasitic capacitance of the terminals and sidewalls. This phenomenon occurs near the pinch-off voltage of the device and results in a drop in the capacitance and a significant increase in the series resistance. These are depicted in Figure 6.4. In MESFET-model-based varactor models these phenomena are not correctly modeled nor can they be included into a simple SPICE-type diode model. A specific varactor model is thus needed for a Schottky varactor. One such is presented in [6.7].

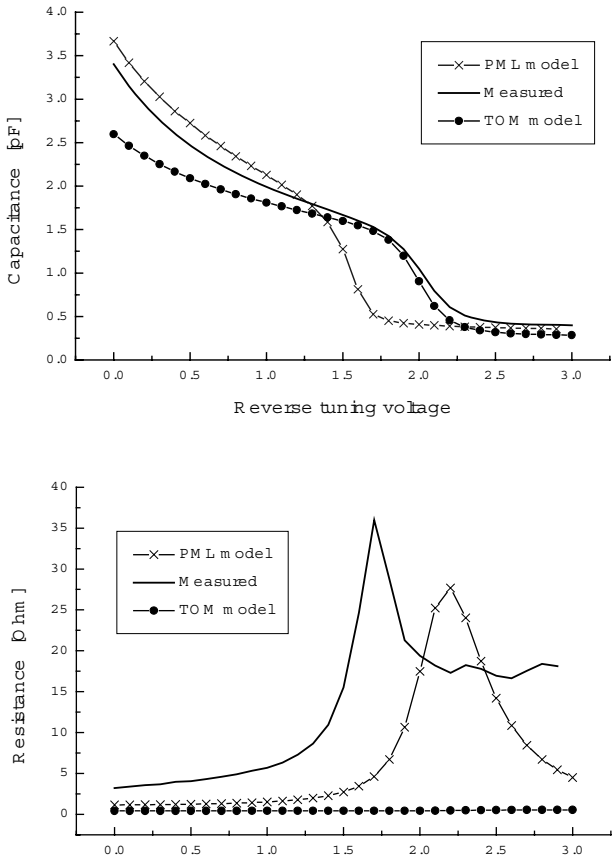

Figure 6.4. Varactor capacitance and series resistance vs. reverse tuning voltage. The test device is fabricated with a 0.7-µm GaAs MESFET technology. The PML model refers to a specific varactor model provided by the foundry and the TOM model is a MESFET model [6.8]. Near the pinch-off at 2 volts the capacitance drops and the series resistance increases.

6.3 Pn-Junction Varactor

In all silicon IC processes pn-junction diodes are available. There are two types of capacitance associated with pn-junctions. The depletion-layer capacitance is associated with the space charge of the impurity atoms, and it dominates in the reverse-biased region. The diffusion capacitance is associated with the charge storage of the free charge carriers, and it dominates under forward bias. Once again, the levels of foundry-supported device models vary significantly. Some foundries provide a basic SPICE-type diode model, which can be used in circuit design but may be inaccurate for RF design. Some RF-dedicated foundries provide actual pn-junction varactor diode models. In some bipolar processes only a bipolar transistor model is provided, and the end user must utilize this as a substitute for an actual pn-junction varactor.

A BJT can replace a varactor in different configurations. We may use a base-emitter junction, base-collector junction, or both. The device layout, and particularly the base and emitter structure, impacts on the BJT-based varactor performance, and hence a comparison should be carried out to find the best alternative. According to simulations for a *VTTB8* BJT, the variant with both the collector and emitter connected has the largest capacitive tuning range. On the other hand, the structure utilizing only the base-collector junction has higher quality factor. Since the BJT layout is not optimized to be used as a varactor, the quality factor is lower than for a real pn-junction varactor. Measurement results concerning this issue are given in Table 6.2. Finally, it is worth pointing out that since the device modeling is done for the actual transistor action, the typical optimization-based methods results in the facts that the secondary parameters may be inaccurate. Therefore, both the Q-value and capacitance may be incorrect.

An actual pn-junction varactor diode is almost invariably implemented as a p^+ n-well junction and, furthermore, n^+ rings are used to strap the n-well to lower the series resistance. The loss of a pn-junction varactor is dominated by the n-well spreading resistance, typically of the order of 1 kΩ/square. Minimum losses are achieved by minimizing the signal path in the n-well. By looking at Figure 6.5 it can be understood that the capacitance units beneath the depletion layer have a longer signal path than the sidewall units. Thus, one should maximize the sidewall capacitance, which is equal to maximizing the perimeter/area ratio. Once again, this is an issue well known by the GaAs community for a long time, and in mm-wave designs circular Schottky diodes are used. In Si ICs one can also favor a concentric (island-type) layout instead of typical comb-shaped (finger-structure) layout; see Figure 6.6. The concentric layout also offers easy and accurate scalability. The drawback of the concentric layout is the large parasitic capacitance from the cathode (n-well) to the substrate. This limits the usefulness to applications where the cathodes are at signal ground nodes. Furthermore, in the concentric layout the anode interconnections result in additional parasitic capacitance, thus reducing the tuning range. In the finger-type layout the above argumentation leads to favoring fingers of the minimum length. In both structures interconnection-related losses should also be kept in mind when one is seeking out the best layout.

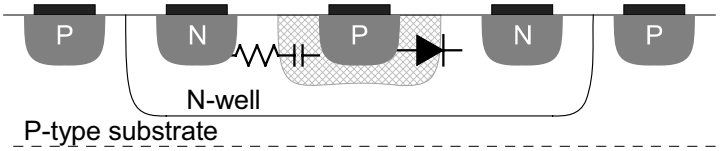

Figure 6.5. Structure of a pn-junction varactor.

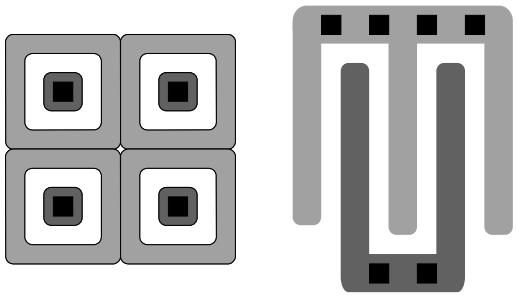

Figure 6.6. Basic layout types for a pn-junction varactor. On the left is the concentric (island-type) layout, and on the right is the comb-shaped (finger-structure) layout.

Pn-junction varactors suffer from a relatively small tuning range, particularly if only a small tuning voltage range is in use. Equation 6.2 gives the capacitance of a reverse-biased pn-junction. Then, the tuning range of the capacitive is

$$\frac{C(V_1)}{C(V_2)} = \left(\frac{V_{BI} - V_2}{V_{BI} - V_1} \right)^{\gamma} \tag{6.3}$$

The built-in potential is given by [6.9]

$$V_{BI} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2} \right) \tag{6.4}$$

Thus, the tuning range of the capacitive is defined by the doping profile (grading coefficient γ) and the doping concentrations N_A and N_D. An end-user is not able to affect these. The only task that exists is to minimize any additional parasitic capacitance, which would further reduce the capacitance range.

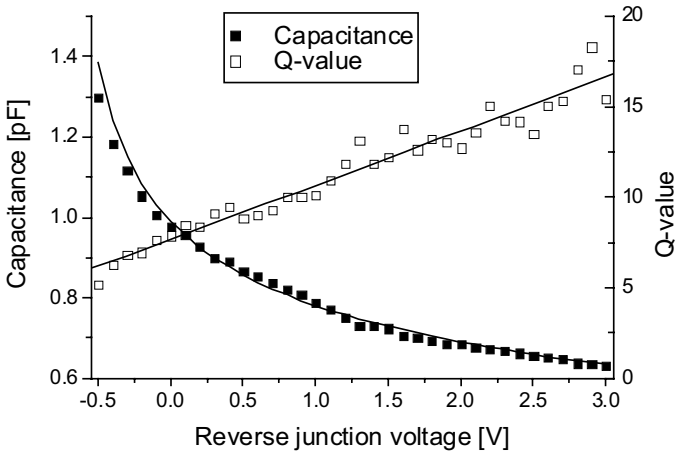

Figure 6.7. Capacitance and Q-value at 2 GHz of a pn-junction varactor vs. tuning voltage. The continuous curve represents Eq. 6.2 with V_{BI}=0.7 and γ=0.27. The test device is a BJT with collector and emitter tied together, fabricated in the *VTTB8* process.

Another aspect worth brief discussion is the modeling of the capacitance of the varactor on the diode forward-bias region. When the device is well reverse-biased both losses and capacitance behave in a well-predictable manner. However, one might consider extending the VCO frequency range by slightly forward biasing the varactor. This is a method known to increase the tuning range significantly but with the penalty of increased phase noise. According to my own experiments, an increment of 10 – 20 dB is to be expected. In a slightly forward biased

diode the large oscillation swing will turn the diode on for a fragment of the cycle. Equation 6.2 predicts the capacitance correctly up to $V_{BI}/2$ [6.10], but at higher voltages many models give incorrect results [6.10],[6.11]. This can be seen from Figures 6.7 and 6.9. In reality the capacitance saturates near V_{BI}. If this forward biasing trick is to be used or if the oscillator has a high voltage swing over a zero-biased varactor, the designer should pay attention to this modeling issue.

I have used a 0.8-µm BiCMOS process (*VTTB8*) for designing some RF oscillators. Since the foundry does not offer any varactor or diode models, I performed some device characterization and layout optimization of my own. This work was presented in [6.12]. The foundry did provide a bipolar transistor model (Gummel-Poon), and such a device was used as a reference varactor. A varactor diode based on 12 parallel unity npn-transistors was fabricated as well as eight different pn-junction diodes as test devices. Figure 6.8 shows a chip microphotograph including typical test structures. The process includes two types of n-wells: an ordinary n-well and a collector-well (c-well). The doping of the latter is chosen to optimize the npn-transistor performance. Furthermore, an ordinary n^+contact layer or a special deep n^+diffusion (sinker) are available. The measurement and parameter extraction results are summarized in Table 6.2. The results clearly indicate the importance of good n^+ contacting. The npn-based varactor has a measured zero-bias capacitance equal to 0.46 pF, the quality factor at 2 GHz is about ten and C_{0V}/C_{-3V} (a 3-V tuning) is 1.52. Correspondingly, the transistor model predicts C_0=0.40 pF, Q_{2GHz}=22, and C_{0V}/C_{-3V}=1.68. In this case the transistor model showed an optimistic performance for the varactor.

Table 6.2. Characteristics of different pn-junction varactors in the *VTTB8* process.

Varactor type	C_{0V}/C_{-3V}	Q_{2GHz}	C/area [aF/µm^2]
npn (CE-B)	1.5	~10	50
p^+ c-well comb-shape, n^+ contact	1.6	~10	140
p^+ n-well comb-shape, n^+ contact	1.6	~20	130
p^+ c-well concentric, sinker contact	1.6	>50	90
p^+ n-well concentric, n^+ contact	1.7	~20	80
p^+ n-well concentric, sinker contact	1.7	>50	80

The second project, which included the testing of some pn-junction varactors, was related to the design of a cable modem receiver. The project will be described in detail in Section 9.3. In this project we used a 0.9-µm SiGe bipolar process from *ATMEL* (previously *TEMIC*). The decision as to whether this project would continue and progress for yet another year was made annually, and therefore from the very beginning we were not focused on actual device development. Instead, in each process run we had some test varactors and inductors similar to those used in the corresponding VCOs. Some general process descriptions can be found in [6.13],[6.14]. Here too two types of pn-junctions were available for use as varactor. P^+-diffusion in a collector-well type diode, used for electro-static discharge (ESD) protection, has a smaller loss and a smaller tuning range, while the base-emitter junction has a higher tuning range, but unfortunately also a higher loss as a result of the polysilicon layer used for the base

region formation. Generally, here both the npn-transistor model and the ESD-diode model proved also to be quite accurate models for use as a varactor.

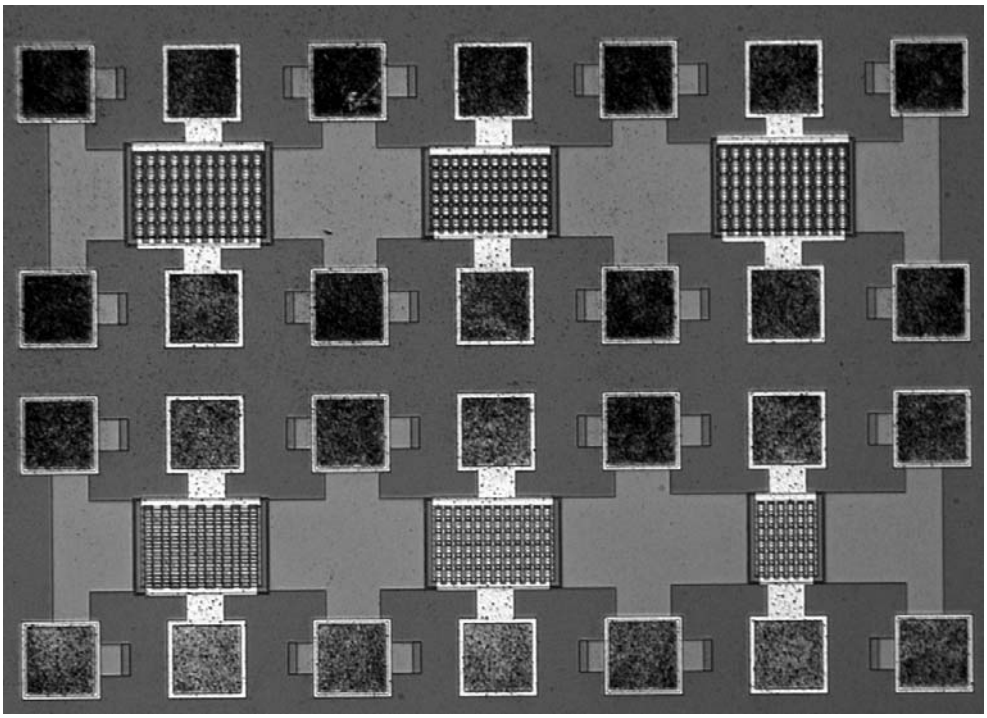

Figure 6.8. Microphotograph of some test varactors fabricated in VTTB8 process.

Altogether nine test devices were implemented and measured. Four were ESD-type, three were BE-type, and two were differential structures. The implementation of the differential structures was motivated by [6.15]. The main issue in different variants of the same type was to study the accuracy of the device scaling and perform some Q-value optimization. The basic characteristics of the test varactors are summarized in Table 6.3, and the tuning curves for seven samples of the last device type are depicted in Figure 6.9. Here we can observe that varactors do have some die-to-die spread, and this is one major source of VCO frequency spread.

Table 6.3. Varactor test devices in ATMEL's SiGe1 process, within five runs.

Test Device	C_{0V} [pF]	C_{0V}/C_{-3V}	Q_{2GHz}	C/area [aF/μm^2]
Two parallel ESD diodes	0.32	1.5	70	150
ESD diode stretched by 2	0.32	1.5	60	180
ESD diode stretched by 3	0.58	1.5	50	190
ESD diode, concentric layout	0.17	1.4	>100	110
ESD diode, differential structure	0.24	1.4	>100	160
ESD diode, differential structure	0.35	1.4	>100	220
BE-diode (npn)	3.9	1.9	10	320
BE-diode (npn) smaller	2.2	1.9	10	240
BE-diode (ripped npn)	1.9	1.9	20	200

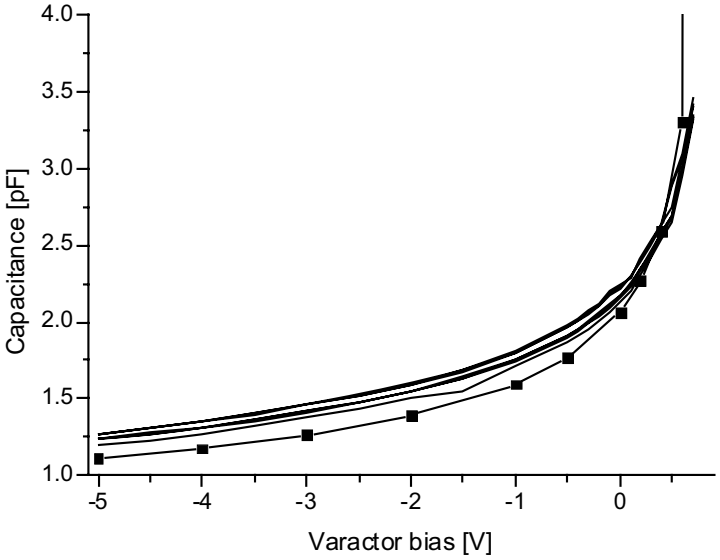

Figure 6.9. Capacitance of the varactor vs. tuning. The curve with square symbols is the model and the black ones are the measured results from seven samples. A 150-fF parasitic capacitance can be added to the model to match the curve to the measured ones. In the positive bias region the matching is poor.

6.4 MOS Varactor

It is a well-known issue that a MOSFET device has nonlinear voltage-dependent gate-to-channel capacitance. Prior to nanometer-scale CMOS technologies MOS varactors were considered impractical because of their low Q-value and strongly nonlinear capacitance tuning curve. Recent studies have shown that both of these problems are obsolete, and MOS varactors have become the most commonly used varactors in recent VCO implementations.

The MOS-varactor capacitance C_{VAR} consists of two parts. The gate oxide results in a constant capacitance C_{OX}, and the capacitive layer in the channel region results in a variable capacitance C_{CH}. The total capacitance is the series connection of these two:

$$\frac{1}{C_{VAR}} = \frac{1}{C_{OX}} + \frac{1}{C_{CH}} \quad \Rightarrow \quad C_{VAR} = \frac{C_{VAR}C_{CH}}{C_{VAR} + C_{CH}} \tag{6.5}$$

As a first look at the MOS varactor, we can consider an NMOS device where the drain, source, and bulk are all tied together, and, furthermore, biased to zero potential. Then, the capacitance-tuning curve, as depicted in Figure 6.10, has three sections. In the accumulation mode the gate voltage is negative ($|V_{GB}| > |V_{FB}|$), and there is a hole surplus in the channel region. The capacitance is equal to C_{OX}. If the negative voltage is reduced, a flat-band situation is reached at the flat-band voltage V_{FB}. Here the channel region is neutral, and fixed oxide and interface charges balance the gate charge. After V_{FB} the device enters the depletion mode. The value of the flat-band voltage V_{FB} is related to fixed impurity charges, and is usually ca. –1V [6.16]. The flat-band voltage varies in different processes, and there is also run-to-run deviation within the same process. Particularly if the gate and well are of the same doping type, V_{FB} is close to 0V [6.17]. In the depletion mode there is a depletion region in the semiconductor, and its depth varies with the potential. Finally, above the threshold voltage V_{TH}, there is a surplus of electrons in the channel, and the channel conducts. The MOS device is in the inversion mode, which is the conventional transistor operation mode, and the varactor capacitance again equals C_{OX}.

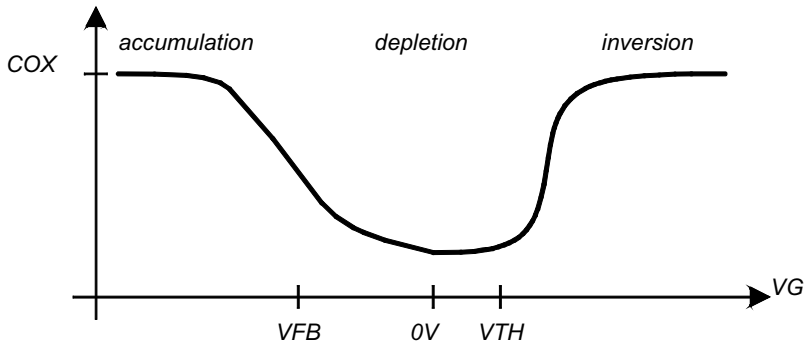

Figure 6.10. Capacitance-tuning characteristics of an NMOS device with B=D=S=0V.

There are four basic types of MOS varactors, as depicted in Figure 6.11. In addition to these four basic types, tuning can be accomplished with back-gate tuning [6.18], a three-terminal accumulation varactor [6.19], or with a gated MOS varactor [6.20],[6.21]. Conventional MOSFET structures result in inversion-mode devices, and replacing the source and drain diffusions with the opposite doping type results in accumulation-mode varactors. In addition to comparing the characteristics of these variants, it is of paramount importance to consider modeling issues once again. Of course, a dedicated varactor model – see e.g. [6.22],[6.23] – is highly desired and supposedly provides good accuracy, but unfortunately only some RF-dedicated foundries provide these models. Often, we have to derive the varactor model from an existing MOSFET model. In the following sections the proper connection type and characteristics of different MOS varactors are presented from the VCO design perspective. Simulations based on a conventional MOSFET model (BSIM3v3.2) and measured results are compared in order to point out how the MOSFET model can be exploited for use as a varactor, and what the accuracy will be. This issue is also discussed in [6.24],[6.25]. The devices are fabricated in a 0.35-μm CMOS process, and measured using on-wafer probes.

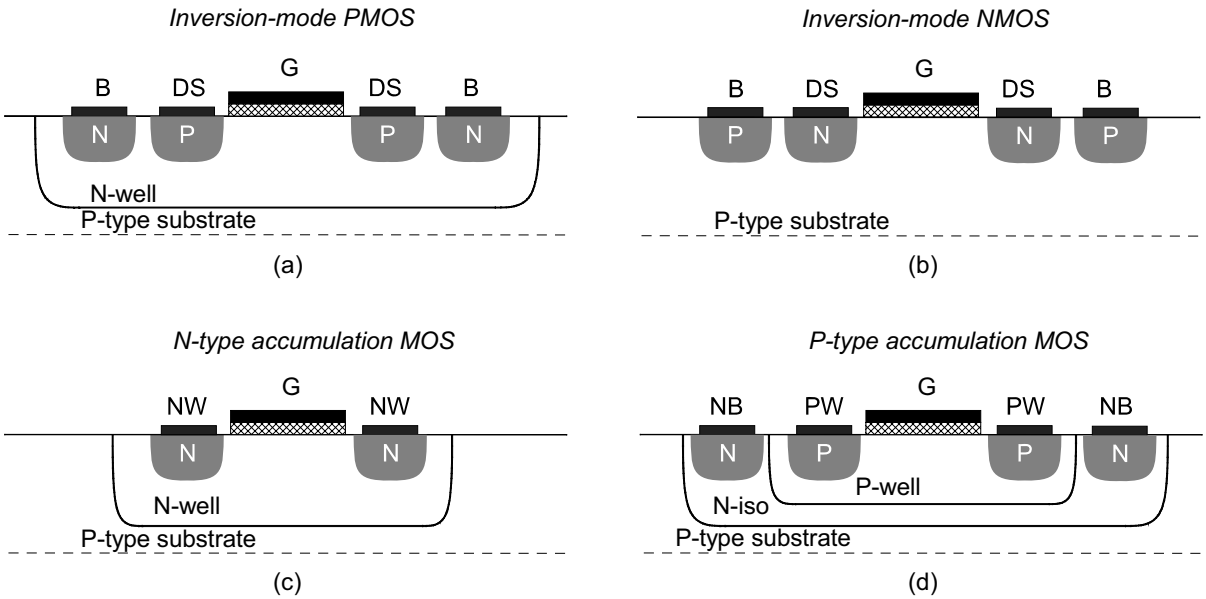

Figure 6.11. Structures of inversion and accumulation MOS devices.

The inversion-mode NMOS varactor in Figure 6.11a is based on the conventional NMOSFET structure. If the gate is connected to the highest potential (V_{DD}) and the DS-node bias is altered, the channel varies from inversion into depletion. In oscillators we connect the gates to the oscillating nodes and the DS-nodes to the tuning node in a differential VCO. The

opposite arrangement is not practical because of the large parasitic capacitance associated with the DS nodes. Figure 6.12 depicts the measured and simulated capacitance curves.

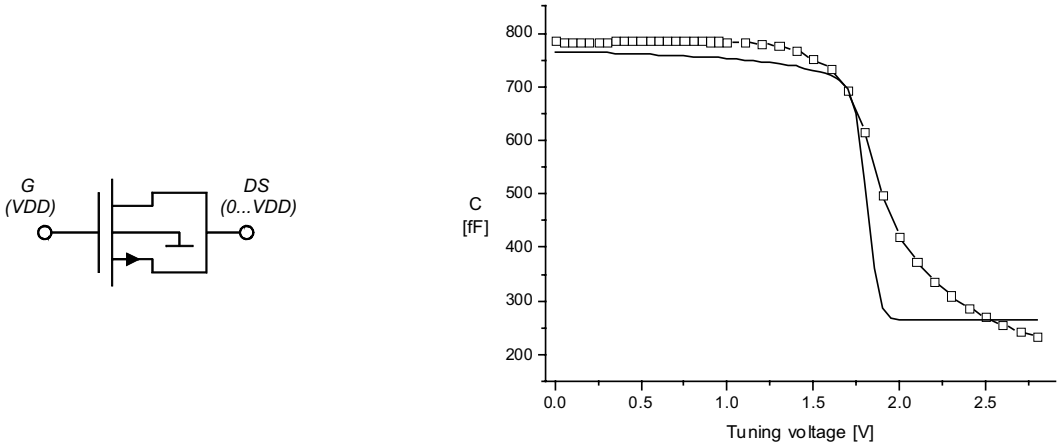

Figure 6.12. Simulated (continuous curves) and measured (square symbols) capacitance of a 56×5.3/0.5-µm inversion-mode NMOS varactor. On the left, the connection of the device is depicted.

The inversion-mode PMOS varactor in Figure 6.11b is complementary to the previous case. Now the gate terminal is connected to zero potential (but not to the signal ground), and the bulk is tied to the highest potential (V_{DD}).

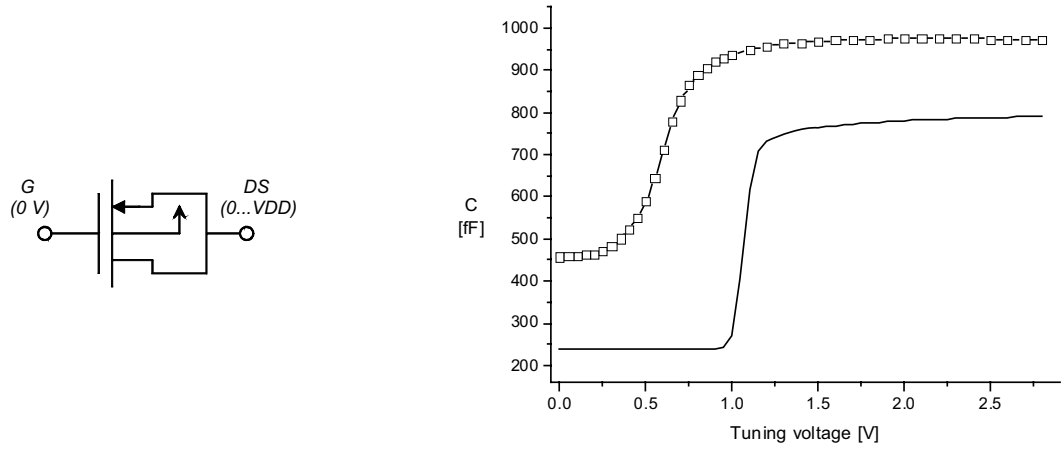

Figure 6.13. Simulated (continuous curves) and measured (square symbols) capacitance of a 64×5.3/0.5-µm inversion-mode PMOS varactor. On the left, the connection of the device is depicted.

The N-type accumulation-mode MOS varactor in Figure 6.11c is established by fabricating N^+-type diffusions into the N-well. Now the well and the polysilicon gate doping are usually of the same type, and hence the flat-band voltage is close to 0V. The device operates in the accumulation and depletion modes. Without P-type diffusions inversion will not take place, and the device remains in depletion even at negative gate-well voltages. This type of MOS capacitor has been known to exist (e.g. [6.26] in 1992), but only in the late 1990s did it become technologically feasible to consider the usage of an RF varactor [6.27]-[6.29]. The N-type accumulation-mode varactor resembles the inversion-mode NMOS device from the circuit design perspective. They can replace each other. The gate terminal is tied to the highest potential.

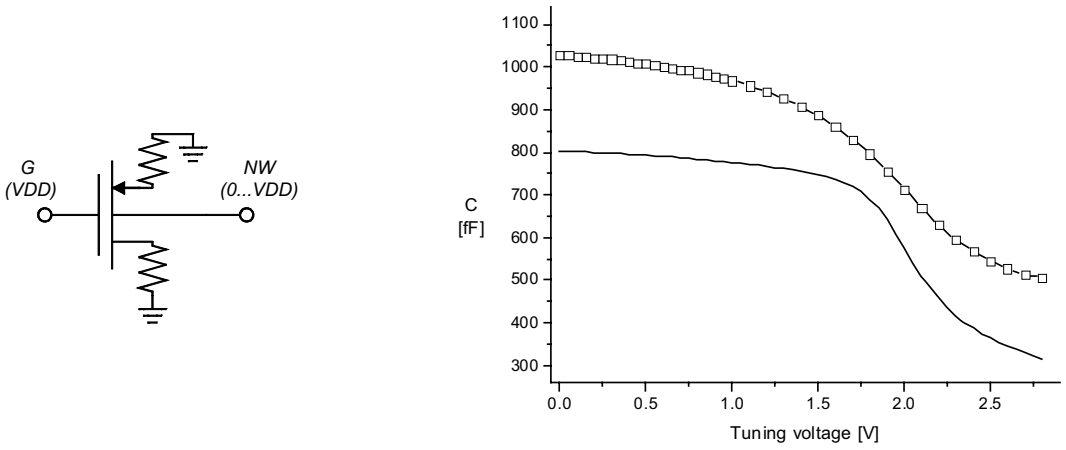

Figure 6.14. Simulated (continuous curves) and measured (square symbols) capacitance of a 64×5.3/0.5-µm accumulation-mode N-type MOS varactor. On the left, the connection of the device for the simulations is depicted. The attached schematic shows how to mimic the device performance with a standard MOSFET model. Ideal noiseless 1-GΩ resistors are used for tweaking the model.

The P-type accumulation-mode MOS varactor in Figure 6.11d resembles inversion-mode PMOS device from the circuit design perspective. They can replace each other. The gate terminal is tied to the lowest potential. This type of varactor is a rare device compared to the previous ones, since it requires an advanced process which offers floating P-wells. Basic "bulk" or "digital" CMOS processes do not have this option. A specific isolation layer (N-iso) is used to separate the P-well from the P-type substrate. The isolation well is usually connected to the highest potential (V_{DD}) in order to provide good isolation. If the supply rail is particularly noisy, the device works still properly, even if the N-iso layer is grounded. The test device here is fabricated in a process lacking this option. It still works properly but only as a stand-alone test device. It draws current from the tuning node into the substrate.

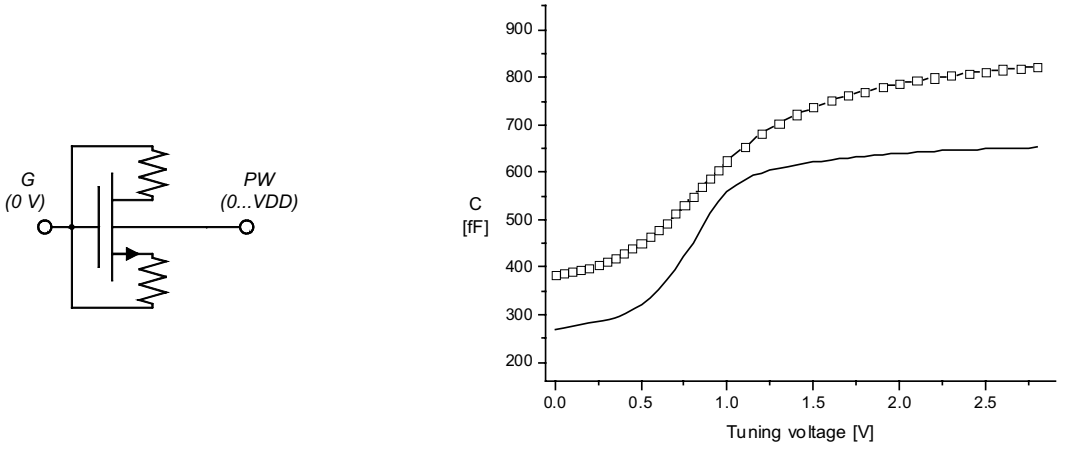

Figure 6.15. Simulated (continuous curves) and measured (square symbols) capacitance of a 56×5.3/0.5-µm P-type accumulation-mode MOS varactor. On the left, the connection of the device for the simulations is depicted.

The position of steep capacitance variation in MOS varactors is related to the gate-bulk voltage. In the previous representations the gates of the N-type devices were biased to V_{DD}, and the P-type devices were correspondingly biased to null potential. This has the result that N-type

devices are used in oscillators with an NMOSFET cross-coupled pair, and correspondingly P-type devices are used with a PMOSFET core. In the CMOS-core implementation the gate bias is at ca. $V_{DD}/2$. Thus, the position of the steep region in the varactor curves is altered but it remains between null and V_{DD}. Hence, in the CMOS case all four variants are feasible.

The previous measurement results show that the BSIM3v3.2 MOSFET model is able to predict the capacitance curve reasonably well. Large noiseless resistors are used in the device modeling to tweak the models for accumulation-type devices. The devices that were measured had slightly larger capacitances in these measurements. The impact of bonding pad capacitances were removed by measuring an open structure, such as one depicted e.g. in Figure 5.10. The impact of the interconnect line from the pad to the device-under-test remains in the final results and it explains the some tens of femtofarads discrepancy given in Table 6.4 in the C_{add} column. Rest of the discrepancy can be explained by process spread. Figure 6.12 shows that the basic inversion-mode NMOS varactor has very small discrepancy between measured and simulated values. So, we may hypothesize that gate oxide (C_{OX}) is close to its nominal value, and the discrepancies are caused by the doping variations in the channel region. These variations cause that the doping density and the profile vary, and this reflects to the channel region capacitance (C_{CH}). Figure 6.13 shows that in the inversion-mode PMOS varactor the threshold voltage has shifted clearly and the capacitance value is larger as well. The N-type accumulation-mode varactor is fabricated into the same type of N-well, and there the capacitance is larger as well. Finally, the P-type accumulation-mode MOS varactor is, unconventionally in this experiment, fabricated into the same type of P-well as the inversion-mode NMOS varactor, and the discrepancy is small. Table 6.4 summarizes these measurements. The quality factors of these devices were significantly lower than what was expected. Usually, in 0.5-µm technologies the quality factors are 2-4 times better than the results here. For convenience, Table 6.5 represents the varactor characteristics of a 0.13-µm CMOS process.

Table 6.4. Measured characteristics of 0.5-µm MOS-varactors in a 0.35-µm CMOS process.

Test Device	C_{max} [fF]	C_{add}* [fF]	C_{max}/C_{min}	Q_{2GHz}	C/area [aF/µm^2]
56×5.3/0.5-µm Inv-mode NMOS	790	70	3.4	10	1000
64×5.3/0.5-µm Inv-mode PMOS	980	210	2.1	10	830
64×5.3/0.5-µm N-type acc-MOS	1030	210	2.0	16	870
56×5.3/0.5-µm P-type acc-MOS	800	80	2.1	10	1000

* C_{add} is the average discrepancy between the measured and simulated curves.

Table 6.5. Simulated characteristics of 0.35-µm MOS-varactors in a 0.13-µm CMOS process. The device models are foundry-provided specific varactor models with tentative status.

Device	C_{max}/C_{min} *	Q_{2GHz}
Inversion-mode NMOS	2.9	40
Inversion-mode PMOS	3.1	50
N-type accumulation-MOS	1.9	120
P-type accumulation-MOS	1.8	60

* Tuning voltage range is 0.2-1.0 V.

A highly simplified analysis of a MOS varactor can be made by assuming that the MOS capacitance is simply area-dependent and only the channel region causes losses. Then we have

$$C = C_{sq}WL \quad and \quad R = \tfrac{1}{4}R_{CH,sq}\frac{L}{W} \quad \rightarrow \quad Q = \frac{1}{\omega RC} = \frac{4}{\omega \cdot R_{CH,sq}C_{sq} \cdot L^2} \tag{6.6}$$

As we can see, the quality factor of a MOS-capacitor is inversely proportional to L^2. The technology scaling thus benefits MOS varactors particularly. In addition, the gate oxide thickness is reduced with the technology scaling, while the actual channel region capacitor does not scale as aggressively. Therefore, the C_{max}/C_{min} ratio for a given L is increased with technology downscaling. However, this seems to be a weak phenomenon. On the other hand, within the same process (constant C_{OX}) more segments with a smaller L have to be connected in parallel to get the same gate area. The parasitic interconnect capacitance is then larger, and results in a degraded C_{max}/C_{min}. A comparison of the tuning range and Q-value vs. L is shown in Figure 6.16 for an inversion-mode NMOS-varactor. This figure is based on a foundry model. and thus it is open to some debate. However, it is in good agreement with the literature survey, and depicts the trend properly.

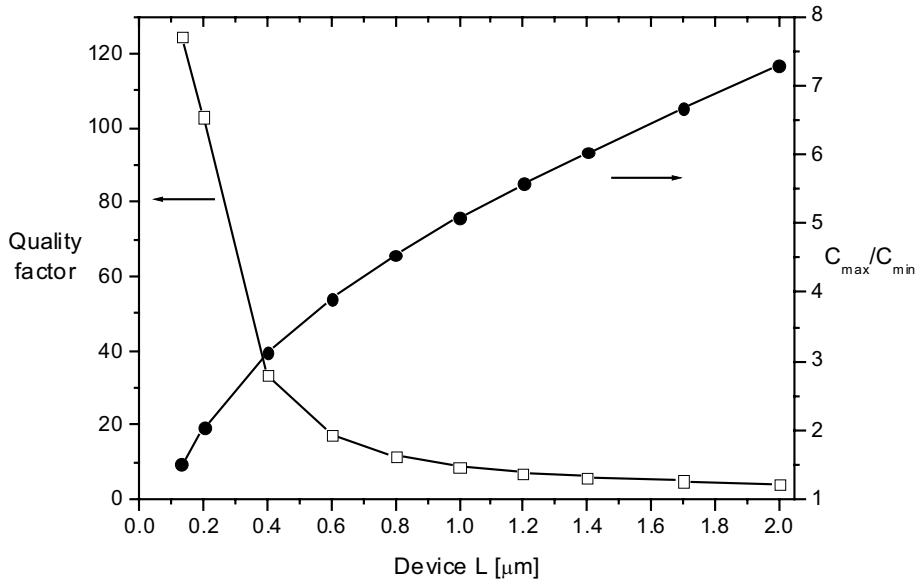

Figure 6.16. C_{max}/C_{min} ratio and minimum Q-value vs. device length L for an inversion-mode NMOS-varactor.

Four segments cause losses in a MOS varactor: 1) metal interconnection resistance; 2) the resistance of the metal contacts to the polygate and diffusions; 3) the resistance of the gate; and 4) the resistance of the well region. The first two can be combined into a constant resistance R_{CONT}, and the gate resistance R_{GATE} also is constant, while the well resistance R_{CH} is variable. Thus, all the losses can be modeled with a single variable series resistance:

$$R_{VAR} = R_{GATE} + R_{CONT} + R_{CH} \tag{6.7}$$

Basic MOSFET models, such as BSIM3v3.2, are useless as a source for varactor loss estimation. They lack terminal resistances and ignore channel resistance when the drain-source voltage is null. Thus, the designer has to implicitly add losses into the model. In practice, a single constant resistance at the gate is most often used. This method, though, does not capture the channel resistance variations during an oscillation cycle, when the varactor mode alters between e.g. inversion and depletion.

The polysilicon gate introduces a constant resistance. For a single gate strip it is given by

$$R_{GATE} = \tfrac{1}{3} \cdot \tfrac{1}{4} R_{sq} \frac{W}{L} \tag{6.8}$$

Here the one-third factor comes from the distributed nature of the structure, and the one quarter factor is gained by feeding the signal from both gate ends. W is actually the length of the resistive strip, and L is the width. Maintaining the analogy to conventional MOSFET terminology causes this contradiction in symbols. R_{sq} is the sheet resistance of the polysilicon layer. Shortening the individual gate strips can reduce the contribution of the gate resistance to overall losses. This means that the device is constructed from several parallel fingers. However, if the fingers are very short, the contribution of interconnection parasitic capacitance to the overall capacitance is increased, and the C_{max}/C_{min} ratio is reduced. Thus, once again we have a trade-off between the tuning range and Q-value.

Resistance values for the metal1 - diffusion contacts, as well as interconnect metal sheet resistances, are often provided by the foundry, and it is thus possible to write a simple analytical geometry dependent formula for the value of R_{CONT}.

The modeling of the channel region resistance is problematic. As already stated, basic MOSFET models completely miss this resistance. Second, it varies, depending on the operation mode. The simple model proposed in [6.30] considers the sheet resistance of the well region:

$$R_{CH} = \tfrac{1}{4} R_{well,sq} \frac{L}{W} \tag{6.9}$$

The problem here is that the sheet resistance of the well is not necessarily known, and it is a constant value. A second method [6.31] extends the previous model by replacing the $R_{well,sq}$ by the resistivity of the well and the thickness of the depletion layer. Andreani [6.32] makes use of linear I_{DS}-V_{DS} characteristics to approximate the channel resistance.

$$R_{CH} = \left(12 \cdot k_p \frac{W}{L} (V_{BG} - |V_T|) \right)^{-1} \tag{6.10}$$

This model suggests that the Q-value has a linear relationship to the overdrive voltage. Soorapanth [6.27] proposed significantly more advanced formulas for accumulation devices. His method has not gained popularity, probably because of its intricate nature. Even in the doctoral thesis of Maget [6.33], she did not propose a closed-form equation for the losses in the channel region, although the thesis mainly focuses on MOS varactors. In device models provided by foundries it seems that measurement-based non-physical fitting parameters are exclusively used in the modeling.

To gain some practical insights into this matter of loss modeling, let us consider losses in the 0.5-µm MOS varactors presented previously. According to the data provided by the foundry, and Equations 6.8 and 6.9, a single 5.3/0.5-µm finger has R_{GATE}=9 Ω and R_{CH}=70 Ω, and the drain-source diffusion resistance is 2 Ω. The total single finger resistance is about 80 Ω, and the corresponding capacitance is 14 fF. This results in Q_{2GHz}=70. The measured devices had a significantly lower Q-value, indicating that this simple calculation is not accurate. The devices had either 56 or 64 fingers, thus the total calculated series resistance is about 1.5 Ω. A specific problem here is that in on-wafer probing the aluminum pads are covered with native oxide, and the probe heads are not necessarily able to completely break it. This results in that there is an additional series resistance in the measured data. It varies in each contact and therefore it cannot be removed. Instead, an uncertainty of some Ohms remains. In Figure 6.17 measured

resistances are shown. Inversion-mode devices have a low resistance in the depletion region; there are resistance peaks in the transition region, and the resistance remains flat and higher in the inversion region. Shape of these curves is similar to what can be found from open literature and models provided by foundries. N-type accumulation-mode varactor shows a low and almost flat series resistance. Most probably, here a constant series resistance caused by probe pad contact and interconnections overwhelms the variable well-resistance. The P-type accumulation-mode varactor has an unexpected shape of the resistance tuning-curve. It might be that since here we have a large mA-range leakage current, it may somehow disturb the device. As explained earlier, with this technology this device is not a feasible one. The results of these experiments leave some open questions, but it would have required a new process round to fabricate more devices to be able to further explore these details with this technology.

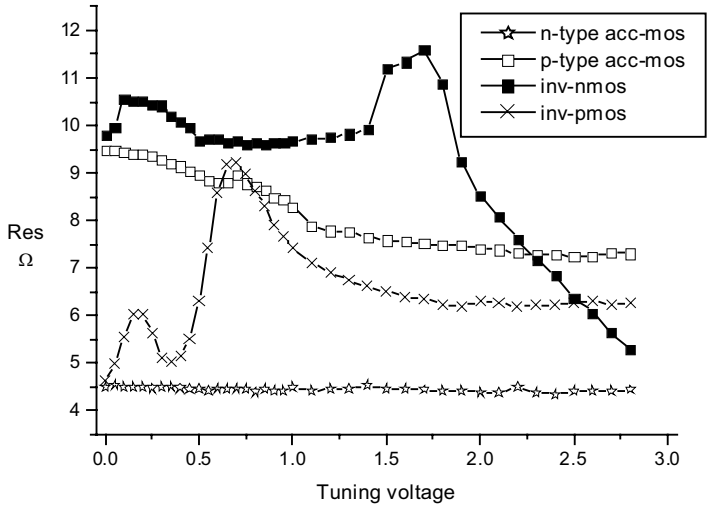

Figure 6.17. Measured series resistances for four 0.5-µm CMOS varactors.

The final question on the topic of MOS varactors is: which one of these MOS varactor types is the best? Unfortunately, the answer to the question is both process- and application-dependent. A design engineer has to carry out a comparison to find the best device for the given technology and task. Nevertheless, in recently published implementations of typical CMOS-VCOs (average tuning range and quite low phase noise), accumulation devices are often preferred. They often provide sufficient capacitive tuning, have a higher Q-value, and are not as strongly nonlinear as the inversion-mode MOS varactors.

6.5 Switched Capacitors

A wide frequency tuning range is required in some applications, or we need a wide tuning range to overwhelm process spread. In such cases a VCO with a single tuning node has a very high tuning gain, often called VCO gain K_{VCO}, which has a unit of Hz/V. High VCO gain results in high phase noise caused by noise in the tuning node, and the high spurious content of the synthesized LO signal. To tackle this problem, we may divide the tunable capacitor into coarse-tuning and fine-tuning branches. Such an arrangement is depicted in Figure 6.18. As such, the discrete and fine tuning method has been well known for a long time [6.34], but during the era of discrete VCO modules it was not often used because of the increased complexity of the tuning arrangement. Nowadays, in fully integrated PLLs, where the VCO is on the same chip as the rest of the circuits, coarse tuning is widely used. If the tunable capacitors (fine and coarse) are of the same type, we will not gain in terms of the Q-value or overall tuning range by dividing them. Only the VCO gain in phase-locked conditions in PLL

is reduced. However, it is possible to use different types of capacitors for fine-tuning and for coarse tuning. Often, MOS varactors are used for coarse tuning and pn-junction varactors for fine-tuning. A second alternative is to use a linear capacitor and a switch for coarse tuning. This method requires a high-quality RF switch, and thus it is only feasible in sub-micron CMOS technologies.

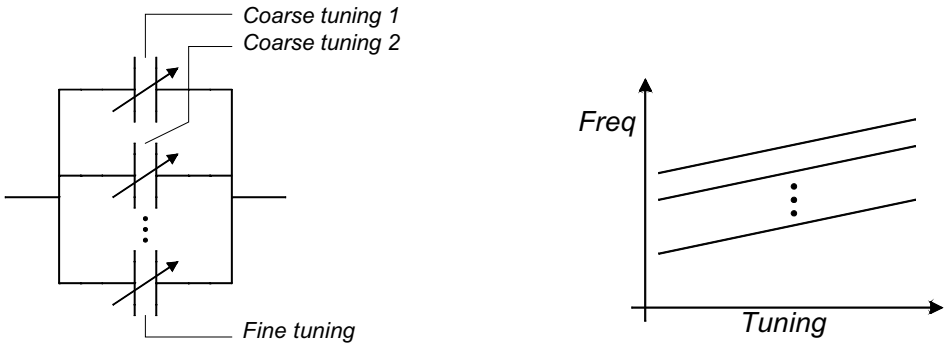

Figure 6.18. (a) A tunable capacitor network can include fine-tuning and coarse-tuning capacitors. (b) The VCO frequency is characterized by a set of discrete overlapping curves.

A switched capacitor (SC) network consists of parallel SC units, usually sized according to their binary weight, i.e., the sizes are multiples of 2^N. An SC unit consists of a linear capacitor and a MOSFET switch. Four basic structures are shown in Figure 6.19. Both single-ended and differential structures were used in early RF IC implementations [6.36],[6.37], but differential structures are favored nowadays. The differential switch is biased with resistors or with tiny MOSFETs depending on the process characteristics. The circuit in Figure 6.19d has two switches and only one capacitor. Here the capacitance size is halved, but the switches are double-sized. In conventional CMOS this gives inferior performance, but in SOI CMOS such a structure can be used [6.37].

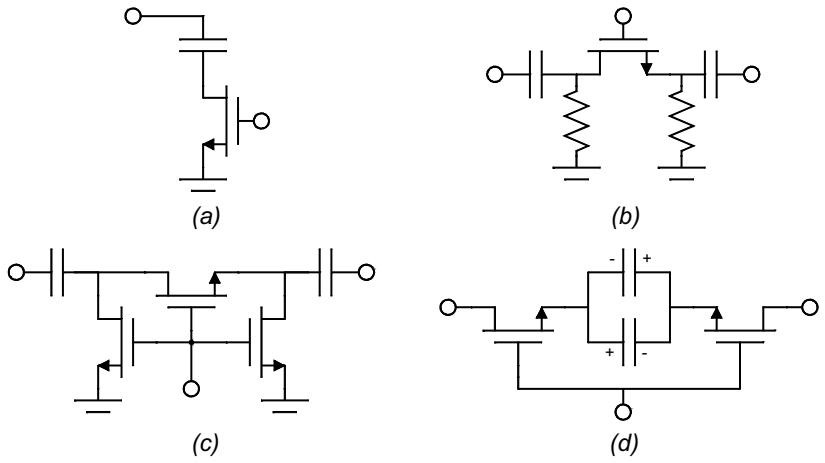

Figure 6.19. Typical switched capacitor units.

The capacitive tuning range and quality factor of the complete SC array are equal to the quality of a single unit. The switch has finite on-resistance and in the off state the model is simply a parasitic capacitance C_{off}. In the on state there are parasitic capacitances as well, but their impedance is far higher than the on-resistance, and therefore they are neglected in the following analysis. The parasitic capacitance in the off state can be approximated with

$$C_{off} = C_u \cdot W \cdot L \tag{6.11}$$

The on-resistance of the switch can be similarly approximated with

$$R_{on} = R_u \cdot L/W \tag{6.12}$$

Here, C_u and R_u are simple coefficients representing the corresponding capacitance and resistance. We want to maximize the quality factor and simultaneously have a high C/C_{off} ratio. This means that we want to maximize the product

$$Q \cdot C/C_{off} = \frac{1}{\omega C R_u \, L/W} \cdot \frac{C}{C_u L W} = \frac{1}{\omega C_u R_u} \cdot \frac{1}{L^2} \tag{6.13}$$

Thus, minimum-length devices give the best performance, and technology scaling improves the performance. However, an SC network still has a limited and often quite mediocre performance. As an example, let us consider a 0.1-pF SC-unit for a 4-GHz VCO in the 65-nm CMOS technology. The quality factor and available capacitance tuning range are depicted in Figure 6.20. If we desire Q=20, the capacitance tuning range is only about 5. Furthermore, in practice the linear capacitor has a parasitic capacitance, which appears in parallel with the switch and causes the capacitance tuning range to deteriorate further.

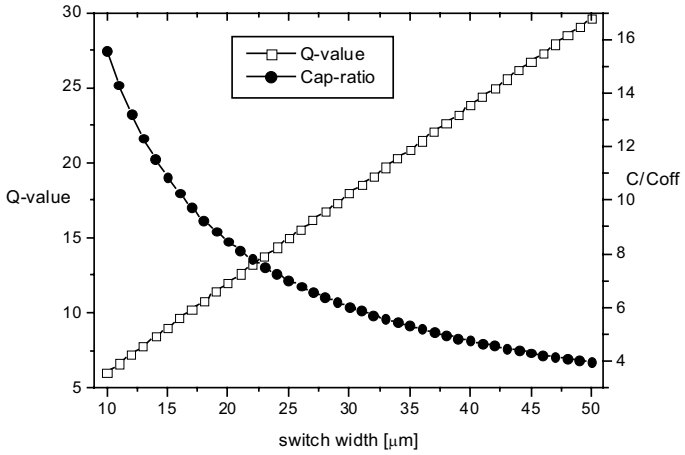

Figure 6.20. Q-value and capacitance ratio for an SC unit vs. switch size. NMOS L=0.1 μm.

Next, we will consider the overall frequency tuning range of a VCO with an SC array. The frequency range is related to the ratio of the maximum and minimum total capacitance:

$$\omega_{osc} = \sqrt{\frac{1}{LC_{tot}}} \quad \Rightarrow \quad \frac{f_{\max}}{f_{\min}} = \sqrt{\frac{C_{\max}}{C_{\min}}} \tag{6.14}$$

The total capacitance in a VCO consists of the varactor capacitance C_{VAR}, the capacitance of the switched capacitor array C_{SCA}, and the parasitic capacitance C_{par}, which is caused by the inductor, negative resistance circuit, and output buffer. The varactor has a tuning range α, and the SC array has the size N and for it C/C_{off} is labeled with β. Thus we have

$$C_{VAR} \in \left[C_V, \alpha C_V\right] \quad and \quad C_{SCA} \in \left[NC_{SC}, \beta NC_{SC}\right] \tag{6.15}$$

The VCO frequency range is now given by

$$\frac{f_{\max}}{f_{\min}} = \sqrt{\frac{\alpha C_V + N\beta C_{SC} + C_{par}}{C_V + NC_{SC} + C_{par}}} \tag{6.16}$$

Next, we define two size-related factors, a and b.

$$C_V = a \cdot C_{SC} \quad and \quad C_{par} = b \cdot C_{SC} \tag{6.17}$$

The tuning range is now expressed as

$$\frac{f_{\max}}{f_{\min}} = \sqrt{\frac{\alpha a + N\beta + b}{a + N + b}} = \sqrt{\frac{\frac{\alpha a}{N} + \beta + \frac{b}{N}}{1 + \frac{a+b}{N}}} \xrightarrow{N\ is\ large} \frac{f_{\max}}{f_{\min}} \approx \sqrt{\beta} \tag{6.18}$$

Typical values here might be: a=b=5,varactor tuning range α=2, SC-unit capacitance ratio β=3, and the size of the SC array N=32 (five units). With these values the above equation gives a tuning range of 1.63, whereas here $\sqrt{\beta} = 1.73$. Thus, even with a modest 5-bit SC array the frequency tuning range is close to the ideal $\sqrt{\beta}$, and with a larger SC array size it is even closer.

The tuning range of the fine-tuning varactor in parallel with an SC array has to be large enough to ensure sufficient overlap of adjacent tuning curves. The amount of overlap required depends on the process characteristics (PVT variations). In practice, the uppermost curves, i.e. the ones with all and all but one SC units off, are the most critical. If sufficient overlap is achieved there, the same applies in the other curves as well. Figure 6.21 depicts the situation.

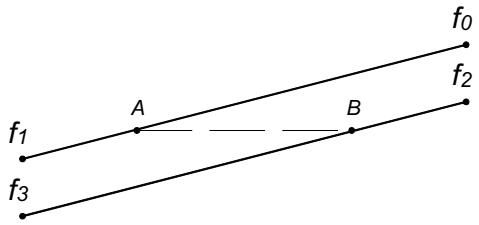

Figure 6.21. Sufficient overlap is needed to guarantee continuous frequency range under PVT variations.

Using the same notations as previously, the frequency f_1 is given by

$$f_1 = \sqrt{\frac{1}{LC_1}} \quad where\ C_1 = \alpha C_V + C_{par} + NC_{SC} \tag{6.19}$$

and correspondingly f_2 is given by

$$f_2 = \sqrt{\frac{1}{LC_2}} \quad where\ C_2 = C_V + C_{par} + \beta C_{SC} + (N-1)C_{SC} \tag{6.20}$$

Now we must have $f_2 > f_1$, and we may define the overlap factor OL by

$$OL = \frac{f_2}{f_1} = \sqrt{\frac{C_1}{C_2}} = \sqrt{\frac{\alpha C_V + C_{par} + NC_{SC}}{C_V + C_{par} + \beta C_{SC} + (N-1)C_{SC}}} \tag{6.21}$$

It is difficult to draw conclusions directly from the above result. In Figure 6.21 points A and B are inside the overall tuning range and are selected to be such that the overlap is sufficient. For these points the factor OL=1, and from (6.21) we get

$$\frac{\alpha_{AB}C_V + C_{par} + NC_{SC}}{C_V + C_{par} + \beta C_{SC} + (N-1)C_{SC}} = 1 \quad \Rightarrow \quad C_V = \frac{\beta - 1}{\alpha_{AB} - 1} C_{SC} \tag{6.22}$$

Here α_{AB} is the tuning range of the varactor inside the tuning range A-B, and C_V also corresponds to point B. This result is not particularly useful, but it shows us that the varactor size is usually in the range of 3-10 times C_{SC}. In practice, this linear analysis is too simple for practical design use and this design phase requires a set of tedious non-linear circuit simulations to find out the proper dimensioning in the presence of PVT variations.

In basic phase-locked loop design the VCO gain is assumed to be constant. However, it varies within a single tuning curve as well as from curve to curve. Particularly in the SC array case, the K_{VCO} variation may cause problems, and thus its variation requires some attention. A simple linear analysis of K_{VCO} resembles the previous analysis of proper varactor sizing. The resulting equations are either not informative, and thus are not presented here. If the variation is unacceptable, the remedy is to modify the capacitance network. Figure 6.22 presents two simple solutions. In [6.38] a more extensive arrangement is presented.

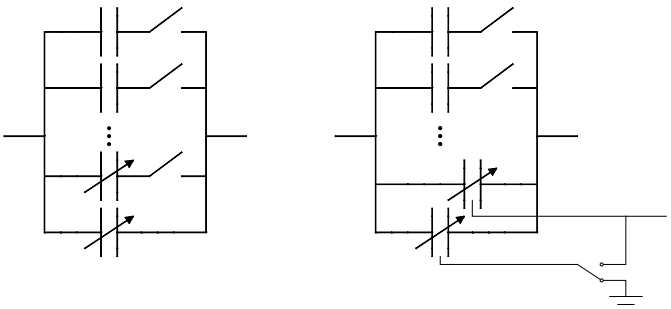

Figure 6.22. Two circuit techniques for reducing the K_{VCO} variation.

Finally, I will present a design example in order to bring some practical insight into this matter. A 5-bit SC array is designed for an 8-GHz VCO. The technology is 65-nm CMOS. Here the minimum size of the linear capacitor supported by the design kit was 25.4 fF. This limitation set one boundary for design and it limited the size of the SC array to 5 units. An N-type accumulation MOS varactor (200x1/0.2 μm) provides a tuning range α=3, and has Q_{8GHz}=30. The SC array itself has a tuning range β=5.5, and has Q_{8GHz}=15. The structure of the actual SC unit is shown in Figure 6.23, and the VCO frequency characteristics are shown in Figure 6.24. The curves are not uniformly distributed. Instead, in transition, where several switches change their state simultaneously, there is a larger shift in capacitance. This problem is most severe with the largest unit (transition 01111→10000) and to diminish this effect, the last unit is of a size 15 instead of 16. This phenomenon is also observed and discussed in [6.39]. In this tuning arrangement the VCO gain varies from 170 MHz/V to 330 MHz/V in the phase-locked situation, and with nominal parameters. This variation was in the acceptable range, and no additional tweaking was needed.

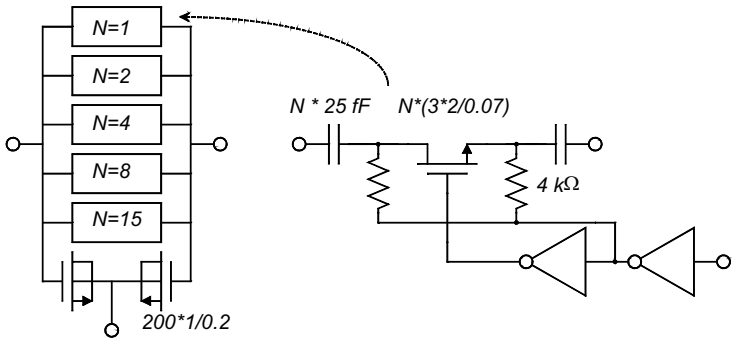

Figure 6.23. 5-bit SC array and N-type accumulation-MOS varactor for 8-GHz VCO.

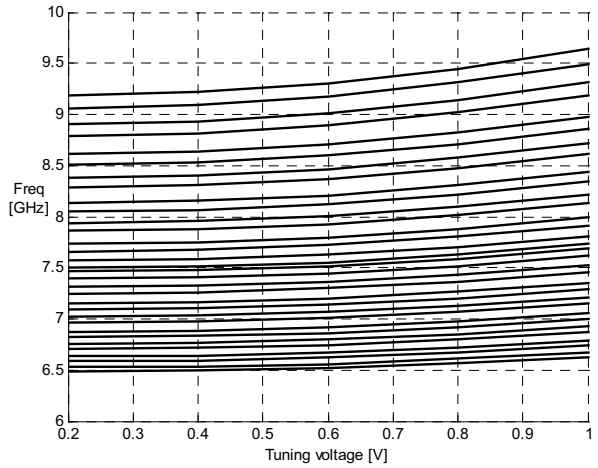

Figure 6.24. VCO frequency range.

6.6 Series and Antiparallel Configurations

A single varactor device can be replaced by a more complicated structure. Figure 6.25 shows the anti-parallel and back-to-back configurations, which are the most common. In addition, combinations of PMOS- and NMOS-type devices are possible in CMOS technologies, or we can use switched varactors. A set of parallel devices can be biased to different values, so that the eventual tuning curve has the desired shape [6.40].

Figure 6.25. Antiparallel varactors on the left and back-to-back varactors on the right.

Series and parallel configurations linearize the tunable capacitor, and they are used to suppress distortion in filters and noise up-conversion in oscillators. Meyer [6.41] analyzes these structures and finds out that the antiparallel configuration is inferior. Bonfanti [6.42] draws the same conclusion with oscillators. Furthermore, the use of an antiparallel structure requires a differential loop filter in the PLL, thus occupying a larger die area [6.43]. In discrete component design the use of back-to-back varactors is a well-known and commonly used method. The configuration does indeed offer lower AM-to-PM conversion, but with the penalty of varactors that are twice as large. In practice, it often turns out that in RF IC cases the improvement is minor, and basic varactor structures are used.

In order to gather some practical experience on this matter, we compare pn-junction and inv-mode PMOS varactors in a PMOS oscillator. Figure 6.26 depicts the oscillator and the alternative capacitor structures. A small signal (1μA) at 100 kHz is injected into the bias current to simulate the AM-to-PM conversion. Table 6.6 includes simulation results. We observe that in the pn-junction varactor cases some improvement is achieved at low offset frequencies when the back-to-back configuration is used, while for the inversion-mode PMOS varactors the basic structure is better.

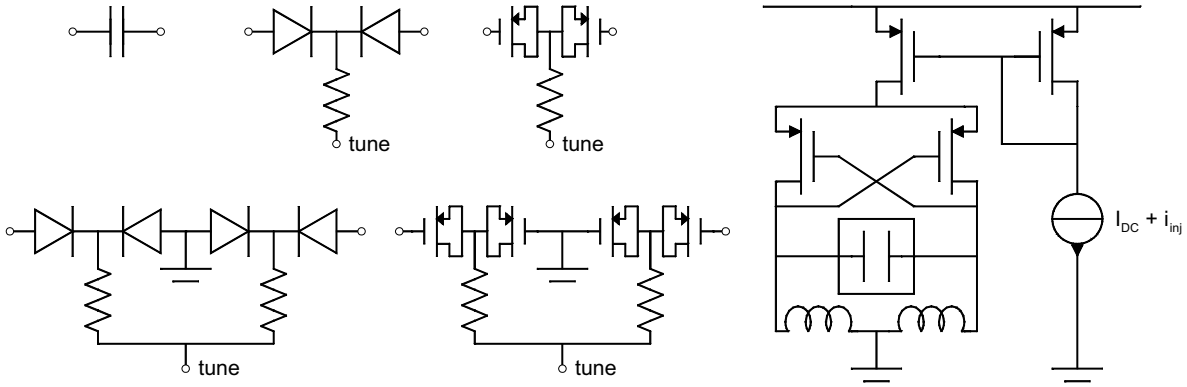

Figure 6.26. On the left, five alternative capacitor arrangements are depicted and on the right is a PMOS CCP oscillator with current biasing. The square block is replaced by one of the capacitor arrangements at a time. The bias source includes an injected interference signal i_{inj}.

Table 6.6. PMOS CCP oscillator characteristics with different capacitors. L=2nH/2Ω, V_{dd}=1.2V. P_{SB} gives the relative strength of the 100-kHz sideband as a result of the injected signal.

Case	Freq [MHz]	TR%	P_{SB}* [dBc/Hz]	$\mathcal{L}$(1kHz)* [dBc/Hz]	$\mathcal{L}$(1MHz)* [dBc/Hz]
Linear capacitor, C=0.65pF	3000	-	-42	-37	-123
Pn-junction varactors	2870-3310	14	-18	-17	-106
Back-to-back pn-varactors	2860-3250	13	-26	-28	-105
Inv-mode PMOS varactors	2710-3370	22	-20	-22	-111
Back-to-back PMOS-varactors	2710-3350	21	-20	-24	-102

* Worst value within the tuning range 0 … 1.2V

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7 Oscillators Based on Artificial Reactive Elements

As discussed in the previous two chapters, the passive elements in integrated circuits suffer from poor performance. Variable capacitors have a narrow tuning range and inductors have a low Q-value. Particularly prior to modern deep sub-micron CMOS technologies, these problems were severe and no good remedy was known. Even in mid-1990s it was still not at all clear whether the RF CMOS circuits would ever become feasible, and, for instance, the idea of having a high-quality switched capacitor network for the coarse tuning of an LC-VCO was just a dream. There was therefore a strong motivation to seek out alternative methods to implement high-performance reactive elements. Active circuits can be used to emulate reactive elements. As long as we ignore the noise and large-signal characteristics and just study these circuits using simple analytical expressions or with small-signal circuit simulations, these circuits possess deceptively attractive characteristics, such as a high quality factor or wide tuning range. In reality, the high noise and small dynamic range severely limit the use of these circuits. This is a fundamental limitation of all integrator-based active circuits [7.1]. Although nowadays a wide set of papers on these circuits exists, and they rarely, if ever, show good performance, these circuits still pop up from time to time because of their seductive nature.

Active inductance oscillators, and two types of tunable active capacitor oscillators are discussed in this chapter. Prior to them, we study an artificially Q-enhanced inductor and a corresponding Colpitts oscillator to provide a smooth transition into the subject.

7.1 Artificially Q-Enhanced Inductor

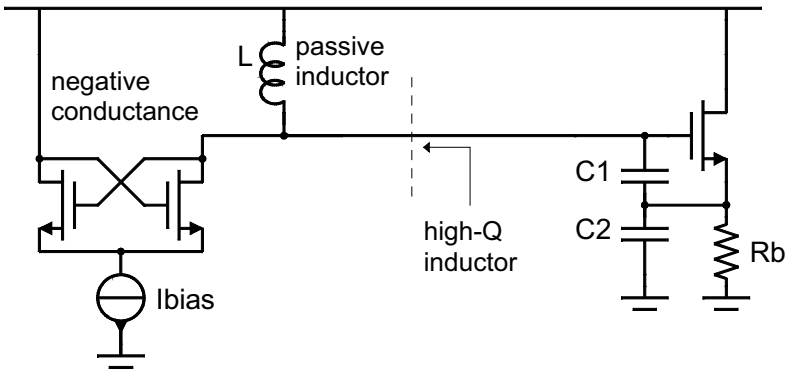


Figure 7.1. Colpitts oscillator with artificially Q-enhanced inductor.

Figure 7.1 depicts a common-drain Colpitts oscillator. Here a cross-coupled transistor pair is used to generate the negative conductance G_{neg}, which appears in parallel to the inductor and will partially compensate for the losses of the inductor. The parasitic capacitance caused by the CCP can be embedded to C_1-C_2. In the small-signal analysis the inductor seen by the actual oscillator is a high-Q device. The Q-value of the Q-enhanced inductor is

$$Q_{L,enh} = \frac{1/\left(G_{pass} - G_{neg}\right)}{\omega L}, \qquad G_{pass} = \left(R_{ind}\left(1 + Q_{pass}^2\right)\right)^{-1} \tag{7.1}$$

Here R_{ind} is the series resistance of the coil and Q_{pass} is the corresponding quality factor. For the 2-nH coil with 2-Ω series resistance, Q_{pass}=19 at 3 GHz and G_{pass}=1.4 mS.

Prior to showing simulations on this matter, we need to consider the definition of the Q-value once again. In nonlinear circuits the signal waveform is always as least slightly distorted and

correspondingly a portion of the energy of the signal is at higher harmonics. Strictly speaking, from the circuit theory point of view, the Q-value is not defined for nonlinear cases. However, we may define the one-port Q-value as before, but now taking into account only the fundamental.

$$Q_{11} = \frac{\left|\mathrm{Im}\{Z_{in}\}\right|}{Re\{Z_{in}\}}, \qquad Z_{in} = \frac{V_{in,fund}}{I_{in,fund}} \tag{7.2}$$

Figures 7.2 and 7.3 depict the quality factor of an artificially Q-enhanced inductor measured at the boundary marked with a dashed line in Figure 7.1. The supply level is 2 V. The quality factor decreases with increased excitation when the CCP bias current is kept constant. However, by increasing the bias current we do achieve the high-Q mode, even in the large voltage swing case.

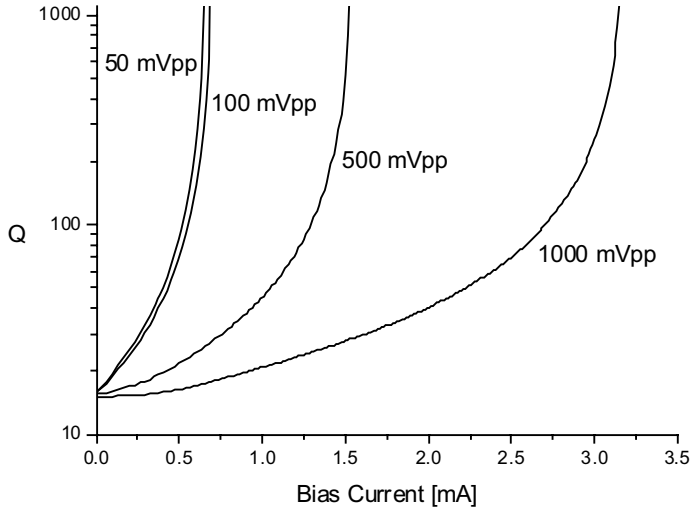


Figure 7.2. Quality factor vs. CCP bias current with four levels of excitation.

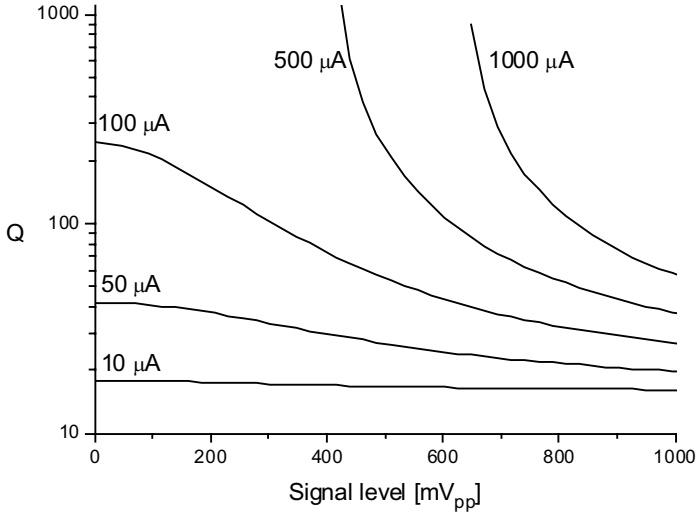


Figure 7.3. Quality factor vs. the level of excitation at five bias current settings.

The quality factor of a Q-enhanced coil decreases with an increased oscillation swing. On the other hand, the oscillation swing increases with the Q-value. Furthermore, the amount of bias current needed for high-Q operation at large excitation exceeds that needed for the onset of oscillation resulting from the CCP alone (i.e. without the Colpitts core). Therefore, in order to

be able to study a case where the high-Q inductor still remains stable by itself, we need to design an oscillator where the voltage swing remains reasonably small. The circuit depicted in Figure 7.1 is modified by adding a by-pass capacitor to separate the inductor and the Colpitts core. A high-value resistor sets the bias level for the gate of the oscillating transistor. A 2-V supply is then used for the CCP and a 1-V supply for the Colpitts core. Table 7.1 presents a set of design cases; first, a conventional Colpitts oscillator with moderate and high Q-value coils, and then the same with corresponding active counterparts. Actually, when the circuits were being simulated, all combinations of bias arrangements were swept through. No improvement in the oscillator performance is achieved with this arrangement in any case.

Table 7.1. Oscillator cases, L=2nH, C1=2pF, C2=6pF, $V_{dd\_Colpitts}$=1V, V_{dd_CCP}=2V
In the two first cases the CCP is not connected, and in the four next cases the CCP compensates Rind. In the last case the Colpitts core is off. Ibias is the bias current of the actual current mirror.

Case	Freq [MHz]	V_{osc} [V_{pp}]	I_{COL} [mA]	I_{CCP} [mA]	$\mathcal{L}$(10kHz) [dBc/Hz]	$\mathcal{L}$(1MHz) [dBc/Hz]
inductor Q=20 Rb=300 Ω	2910	0.70	1.7	-	-71	-123
inductor Q=200 Rb=5 kΩ	2910	0.66	0.14	-	-81	-133
Rind=2Ω Rb=300 Ω Ibias=0	2900	0.68	1.7	0	-71	-122
Rind=2Ω Rb=300 Ω Ibias=100 μA	2890	0.95	1.8	0.37	-54	-113
Rind=2Ω Rb=5 kΩ Ibias=300 μA	2880	0.48	0.13	0.8	-65	-111
Rind=2Ω Rb=5 kΩ Ibias=1 mA	2880	1.35	0.16	1.9	-58	-115
Rind=2Ω Rb= ∞ Ibias=7 mA	2860	3.5	-	7.2	-65	-120

The correct viewpoint on this case is to consider that while the Colpitts oscillator is oscillating the CCP simply feeds additional energy into the resonator and increases the voltage swing. Instead of having a stable high-Q inductor within the Colpitts oscillator we have a situation where two active devices, the CCP and the Colpitts core, provide energy for oscillation. Conceptually, there are two negative conductors and a low-Q LC resonator as depicted in Figure 7.4. This arrangement of distributed negative conductance shows worse performance than single negative-conductance circuits. Instead of the arrangement depicted in Figure 7.1, one may suggest more intricate circuits to compensate for the losses of the passive resonator, but to the best of my knowledge they all eventually fall back to the case studied here.

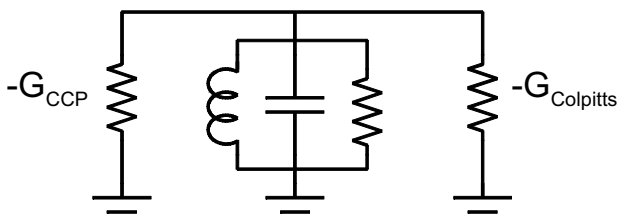


Figure 7.4. The proper conceptual schematic of the circuit in Figure 7.1.

7.2 Active Inductance Oscillators

Active inductors are based on the gyrator principle proposed by Tellegen in 1948 [7.2]. A gyrator performs an impedance conversion and thus it can convert a capacitor to perform as an inductor. One of the first electrical implementations was presented by Bogert in 1955 [7.3], but not until the first transistor circuits emerged did gyrators become feasible electrical elements. There are some examples of early works in [7.4]-[7.9]. Gyrator-based inductors found some room in low-frequency filters but were soon overwhelmed by other techniques, such as switched-capacitor filters. In the late 1980s the enthusiasm for transistor circuit-based inductors grew within the GaAs IC research community [7.10],[7.11], and in the early 1990s many groups worked on these issues [7.12]-[7.30]. Furthermore, a Q-enhancing technique was invented [7.23],[7.26],[7.28]. Active inductance circuits were often FET-only circuits without an explicit capacitor, such as the circuits in Figure 7.5. The operation relied on the parasitic capacitance of the active devices – a method known for its uncertainty. Actually, it even seems that some authors made no clear connection to the under-lying gyrator principle. Later on, the awareness obviously propagated. Little by little the problems of the active inductors, high noise and nonlinearity, became known and research activity decayed. Nevertheless, some good recent works on RF CMOS are presented in [7.31],[7.32]. Moreover, active inductors do find applications in places where their imperfections can be tolerated, such as in active loads [7.33], [7.34].

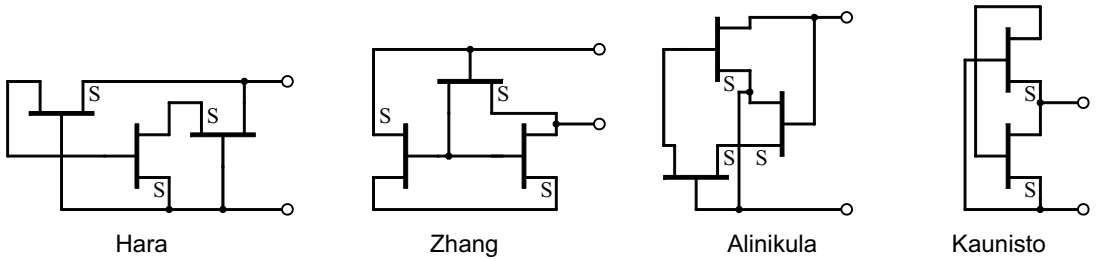


Figure 7.5. Some MESFET active inductor circuits named after their inventors. Here only signal devices are depicted and bias arrangements are not.

7.2.1 Gyrator Principle

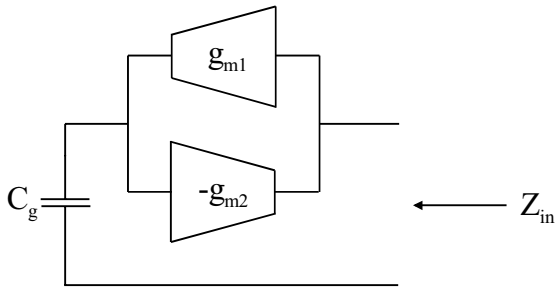


Figure 7.6. Gyrator-based active inductor.

A gyrator is an ideal two-port network element, represented mathematically by

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 0 & -g_{m1} \\ g_{m2} & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{7.3}$$

A gyrator can be implemented with two antiparallel transconductors as shown in Figure 7.6 and it operates as an impedance converter. In principle, the same operation can also be achieved using transimpedance devices, but this duality is not studied further here. If it is assumed that port 1 is terminated with a capacitor C_g, the input impedance for port 2 is then

$$Z_{in} = \frac{j\omega C_g}{g_{m1}g_{m2}} \quad \Rightarrow \quad L = \frac{C_g}{g_{m1}g_{m2}} \tag{7.4}$$

All active inductor circuits follow this kind of relationship regardless of the actual circuit implementation. Note that one of the transconductors can be replaced by a resistor, so we may have single-transistor active inductors as well. The scale of the parameters is worth observing here. If we want to have a typical inductor value of 2 nH, and the gyrator capacitance is chosen to be clearly larger than the parasitic capacitance of the devices, let us say 2 pF, we need $g_{m1}=g_{m2} \approx 30$ mS. If the capacitor is scaled down to 0.2 pF, we still need 10 mS. Therefore, active inductors tend to burn a lot of power.

Next, consider a series resistor R_{gc} for the capacitor C_g. The capacitor has $Q_C = (\omega C R_{gc})^{-1}$ and the corresponding active inductor has an input impedance of

$$Z_{in} = \frac{1}{1+Q_C^{-2}}\left(\frac{\omega C_g}{g_{m1}g_{m2}Q_c} + \frac{j\omega C_g}{g_{m1}g_{m2}}\right) \quad \Rightarrow \quad Q_L = Q_C \tag{7.5}$$

The ideal gyrator transformation preserves the level of the Q-value, and as long as the Q-value is even moderate, let us say above five, it has an insignificant impact on the inductance value.

7.2.2 Q-enhancement of Active Inductor

An ideal gyrator-based active inductor has an infinite Q-value. In the practical implementations of the gyrator the input and output impedances of the transistors introduce a phase error, which causes the performance of the active inductor to deteriorate. The aim of the Q-enhancement is to compensate for these phase errors by intentionally adding a tunable phase shifter. Eventually, this compensation can tune the actual circuit to a very high, or basically infinite, Q-value. In this analysis we will associate a phase shift with the respective transconductor. Hence, $g_{m1} \rightarrow g_{m1}e^{j\phi_1}$ and $g_{m2} \rightarrow g_{m2}e^{j\phi_2}$. Furthermore, the total phase shift in the gyrator loop is $\phi = \phi_1 + \phi_2$. Now the input impedance Z_{in} can be expressed as

$$Z_{in} = \frac{j\omega C_g}{g_{m1}g_{m2}\left(\cos\phi + j\sin\phi\right)} = \frac{\omega C_g}{g_{m1}g_{m2}}\sin\phi + \frac{j\omega C_g}{g_{m1}g_{m2}}\cos\phi \Rightarrow \quad Q_L = \cot\phi \tag{7.6}$$

Even a small phase error reduces the Q-value significantly, and the basic circuits such as those shown in Figure 7.5 have Q-values less than ten. A tunable phase shifter in a gyrator arrangement can circumvent this problem. It means that the parameter ϕ becomes a tunable one and as can be noticed from Equation 7.6, the resistive part of Z_{in} is zero if ϕ is zero. A tunable RC phase shifter can easily be implemented with a FET operating in the linear region [7.23],[7.26],[7.28]. One such arrangement is depicted in Figure 7.8.

7.2.3 Noise in Active Inductor

A gyrator circuit constructed from two antiparallel transconductors suffers from noise generated by these devices. It is instructive to imagine that in an active inductor the susceptance itself becomes noisy because it includes the impact of the transconductors, in contrast to a passive case where only the resistive elements generate noise [7.16]. In the simplest case the noise associated with each transconductor can be presented as the equivalent input noise voltages $\hat{v}_{gm1}^2$ and $\hat{v}_{gm2}^2$, respectively. In order to be able to convert these noise

sources to just one equivalent noise voltage we need to load the inductor. If we just use a capacitive load, the resulting resonator has an infinite Q-value, and the analysis is not meaningful. A finite Q-value of the active inductor can be set by introducing losses to the gyrator capacitance. However, we learnt from the prior analysis that the gyrator transformation preserves the Q-value, and it is therefore equivalent to simply use a load resistor to represent the finite Q-value of the active inductor. Hence, here we study a parallel LCR resonator. As a first step, the noise sources of the active inductor are represented by a noise voltage source $\hat{v}_{gm1}^2$ and current source $\hat{i}_{gm2}^2 = g_{m2}^2 \hat{v}_{gm2}^2$. Then the total spectral density of the noise voltage over the resonator is

$$\hat{v}^2 = \frac{\hat{v}_{gm1}^2 + \omega^2 L^2 g_{m2}^2 \hat{v}_{gm2}^2}{\omega^2 L^2 R_p^{-2} + \left(\omega^2 LC - 1\right)^2} \tag{7.7}$$

At the resonance frequency this yields

$$\hat{v}^2\Big|_{\omega_0} = Q^2 \left(\hat{v}_{gm1}^2 + \frac{L}{C} g_{m2}^2 \hat{v}_{gm2}^2 \right) \tag{7.8}$$

Finally, we replace the noise sources with a simple input noise source model of a single FET ($\hat{v}_{gm}^2 = 4kT\gamma / g_m$) and we get

$$\hat{v}^2\Big|_{\omega_0} = Q^2 4kT\gamma \left(\frac{1}{g_{m1}} + \frac{L}{C} g_{m2} \right) = Q^2 4kT\gamma \frac{1}{g_{m1}} \left(1 + \frac{C_g}{C} \right) \tag{7.9}$$

For a passive LC-resonator we have

$$\hat{v}^2 = \frac{4kTR_{ind}}{\omega^2 R_{ind}^2 C^2 + \left(\omega^2 LC - 1\right)^2} \tag{7.10}$$

where R_{ind} is the series resistance of the coil. At the resonance frequency this yields

$$\hat{v}^2\Big|_{\omega_0} = 4kTR_{ind}Q^2 = 4kTQ\sqrt{L/C} \tag{7.11}$$

The ratio of the noise level between active and passive resonators is

$$\frac{Noise, active}{Noise, passive} = \frac{Q^2 4kT\gamma \left(\frac{1}{g_{m1}} + \frac{L}{C} g_{m2} \right)}{4kTQ\sqrt{L/C}} = Q\gamma \left(\frac{1}{Z_0 g_{m1}} + Z_0 g_{m2} \right) \tag{7.12}$$

where Z_0 is the characteristic impedance of the resonator.

Noise in active inductors has been discussed earlier, e.g., by Abidi [7.16] and Craninckx [7.30]. Abidi concludes that the total integrated (rms) noise of an active inductor is 2Q times larger than that of the corresponding passive one. An extensive noise analysis of active inductor filters can be found in Kaunisto's doctoral thesis [7.35].

7.2.4 Active Inductance Oscillator Categories

Active inductance oscillators (AIO) can be categorized into two groups:

> the Type I AIO includes a stable active inductor within a conventional LC oscillator.
>
> the Type II AIO includes an active inductor in such an arrangement that the circuit is unstable without an explicit negative resistor.

The type I AIO is structurally quite obvious. The type II AIO actually just consists of transconductors, capacitors, and resistors. Figure 7.7 is a redrawing of the gyrator structure with the emphasis on the oscillator resemblance. It is worth keeping in mind that the inductive behavior of the circuit is just an artificial viewpoint on the structure. Hence, the Type II AIO is actually just a plain RC oscillator. These circuits are known to suffer from poor phase noise [7.36]. To the best of my knowledge, the Type II AIO does not offer any improvement over a conventional RC oscillator in any form of the actual circuit implementation.

The classification of the AIO types is a little problematic. In Section 7.1 the simulations depicted how the Q-value depends on the excitation signal level, and the same behavior appears with the gyrator-based active inductors as well. Therefore, if we want to have a high-Q active inductor within a Type I AIO, we need to design the inductor to have a very high Q-value, and in practice it may become an unstable one, thus being a Type II AIO.

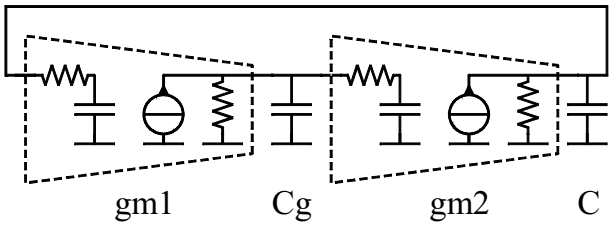


Figure 7.7. Active LC resonator (Type II AIO) redrawn in such a way that it emphasizes its oscillator nature. This circuit oscillates with proper component values.

7.2.5 Circuit Implementations with GaAs Technologies

From 1993 onwards I was involved, in a minor role, in research on active inductor filters [7.20]-[7.24],[7.37], and an obvious part of that work was to consider the use of active inductors in LC oscillators. We fabricated some test circuits that were mainly focused on filter usage, but because of inaccurate device models and other misfortunes, the AIO implementations were not really a success story. Moreover, we learnt quite quickly that active inductors are really noisy and cannot be used as replacements for high-Q inductors in LC oscillators. Therefore our enthusiasm waned, and circuits with solved problems were not re-fabricated. Next, one Type I AIO circuit and one type II AIO circuit are described as examples.

Figure 7.8 depicts a Type I AIO in a 0.5-µm GaAs MESFET technology. The active inductor is based on the circuit by Kaunisto (the rightmost circuit in Figure 7.5). The transistors M_2 and M_3 form a gyrator, M_1 is a tunable current source, and M_T is used for phase compensation for achieving high-Q operation. C_G is the gyrator capacitance. The rest of the capacitors and resistors are used for biasing purposes only. The oscillator is a conventional Colpitts oscillator and the output buffer with high input impedance is used to match the circuit to an external 50-

Ω load. This circuit was designed using fairly inaccurate MESFET models. It turned out that the MESFET model that was applied predicted an incorrect output conductance (g_{ds}). As a result, the active inductor did not operate properly with the original 5-V supply voltage and it had to be increased to 10 V for proper functionality. As can be seen from the circuit schematics the gate biasing of the oscillating FET M_{osc} comes directly from the active inductor. As this voltage was increased, the gate-to-source voltage of M_{osc} became very high regardless of the supply voltage of the oscillator. The result is that the gate-to-source diode of M_{osc} opens up and prevents the proper operation of the transistor. Therefore, this circuit did not oscillate in the measurements. The simulated tuning range is 1.95 - 3.65 GHz.

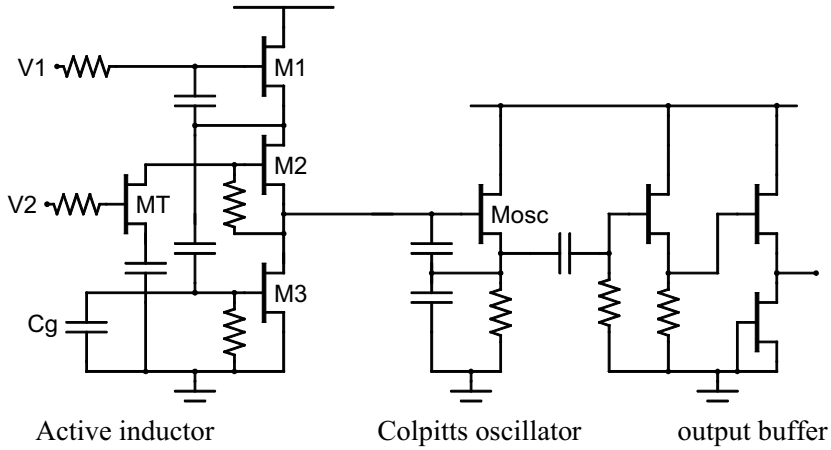


Figure 7.8. Colpitts oscillator with tunable high-Q active inductor.

A GaAs HBT active inductor filter is reported in [7.37]. This high-Q active inductor filter consists of three resonators and small coupling capacitors. We were able to cut the interconnections of two of the resonators on the die, thus achieving a single active high-Q resonator. Its schematic is shown in Figure 7.9. Its structure and functionality is essentially the same as for the circuit in Figure 7.8. This active inductor can generate a reasonable amount of negative resistance to compensate for losses. Accordingly, we were able to get this circuit to resonate straight to a 50-Ω load and operate as a Type II AIO. The supply voltage was 3 V and the circuit consumed about 10 mA of current. The best tuning characteristics were measured with V_{bias}=2.5 V and V_{tune}= 0.5 – 3 V. The measured tuning range was from 2.1 GHz to 2.5 GHz. Typically, the phase noise was around -70 dBc/Hz at a 1-MHz offset from the carrier, measured directly with a spectrum analyzer.

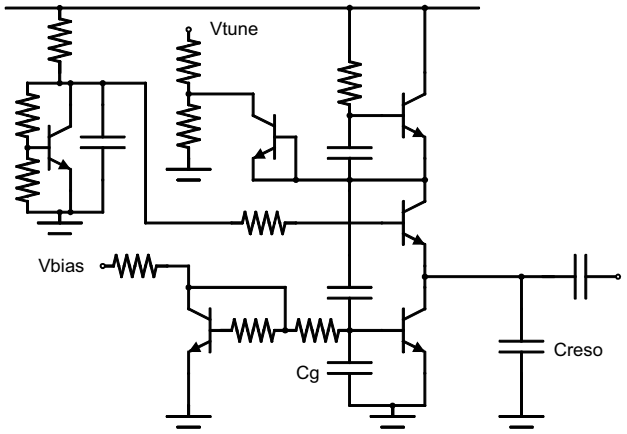


Figure 7.9. Type II AIO with GaAs HBTs.

7.2.6 CMOS Circuit Examples

Here I present some active inductor oscillators designed for a 0.13-μm CMOS technology to show the typical characteristics of CMOS AIOs, to point out the design challenges, and to offer a fair comparison to other types of oscillators.

Case 1: CCP oscillator with active inductor loads

The differential circuit depicted in Figure 7.10 consists of two low-voltage active inductors and a simple cross-coupled pair that is used to generate a negative conductance. The gyrator includes an inverting PMOS stage and a non-inverting NMOS stage. The resistor Rfb boosts the inductance value slightly. The tunable ideal capacitors Cg and Cv are here assumed to have a tuning ratio of 2:1. Table 7.2 summarizes the simulation results. This active inductance oscillator operates over a wide tuning range, but the maximum oscillation frequency is quite low as a result of the resistive boosting technique.

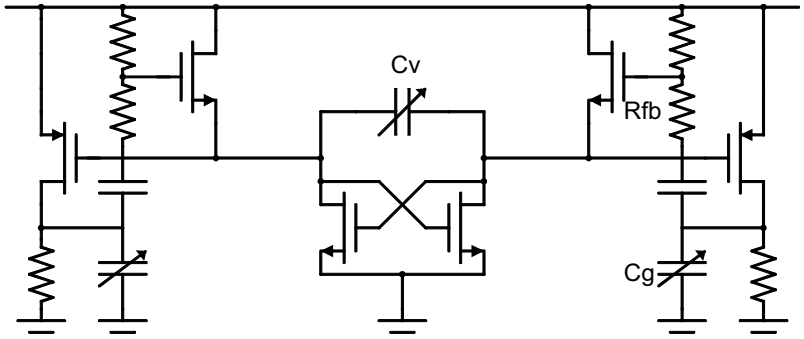


Figure 7.10. Oscillator with low-Q active inductors and CCP negative resistor.

Table 7.2. Performance summary for the above circuit. The technology is 0.13-μm CMOS, the supply voltage is 1.2 V, and the capacitors Cg and Cv have a tuning range 2:1.

Frequency range	740 – 1350 MHz
Current consumption	4.8 – 6.2 mA
Phase noise @ 1 MHz	-80 – -83 dBc/Hz

Case 2: Type II AIO

Active inductor structures do not match well with the low-voltage CMOS technologies. Many topologies require the stacking of three or four transistors, and the circuits do not work at all with a low supply level, or the signal headroom remains very small. In the first design case this was solved with the use of PMOS and NMOS devices. Alternatively, the non-inverting transconductor can be made of two common-source devices in series [7.38]. Such a Type II AIO is depicted in Figure 7.11. This circuit can operate at a low supply voltage ($V_{supply}>V_{TH}+V_{DS}$). The transistor M1 is the inverting transconductor, the devices M2 and M3 form the non-inverting transconductor, and here the active load M4 is used for simple biasing. The bias current Ib and the corresponding current mirror are used to tune the circuit. This circuit arrangement is such that while the bias current Ib is altered, the transconductance of M1 and of M2 and M3 scale into different directions, and the overall product changes only slightly. Therefore, the bias current mainly tunes the Q-value, and varies the inductance value just a little. The gyrator capacitance Cg actually stabilizes the circuit, and therefore for Type II AIO use it is simply omitted. A 200-fF capacitor Cres is set to resonate with the active inductor. Table 7.3 summarizes the performance of this oscillator.

Table 7.3. Performance summary for Type II AIO circuit in Figure 7.11.

Frequency range	4.7 – 5.0 GHz
Current consumption	2.3 – 3.2 mA
Phase noise @ 1 MHz	-65 – -68 dBc/Hz

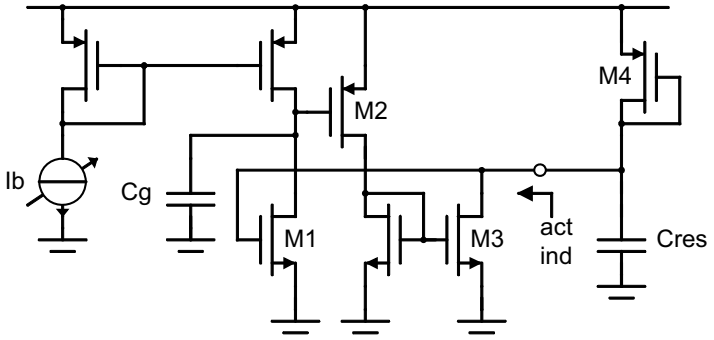


Figure 7.11. Type II AIO circuit.

Case 3: High-Q Type I AIO

The previous active inductor, shown in Figure 7.11, has high-Q operation in the frequency range 3.6 – 4.7 GHz, while the bias current Ib is swept within 0.2 – 1.0 mA. We may establish an oscillator that comprises two such active inductors and a PMOS CCP. In other words, the M4 active loads are simply replaced by a cross-coupled pair. By sweeping the bias current and altering the value of the resonating capacitor, one may browse the parameter space and cover a frequency range wider than just the high-Q region. In all these simulations the phase noise varies within -70 …-80 dBc/Hz at a 1-MHz offset. Therefore, the circuit does not show any attractive phase noise performance although a high-Q active inductor is used. Instead, it is better to use a low-Q inductor by increasing the size of the gyrator capacitance to achieve lower phase noise and a wider tuning range. Table 7.4 summarizes the performance of an oscillator where the active inductors include 100-fF gyrator capacitances, and the resonating differential capacitor is 200 fF.

Table 7.4. Performance summary for Case 3 low-Q circuit.

Frequency range	2.1 – 3.0 GHz
Current consumption	5.4 – 7.3 mA
Phase noise @ 1 MHz	-78 – -84 dBc/Hz

Case 4: Pseudo-differential ring oscillator

Active inductance oscillators may operate as narrow tuning-range devices, or they may have wide bandwidth, typically covering about one octave. Correspondingly, they should be compared to alternative circuits providing such characteristics. Previous chapters have dealt with narrow-tuning-range LC oscillators, and now here we will briefly study a wideband oscillator. A three-stage pseudo-differential ring oscillator, depicted in Figure 7.12, has good characteristics, and on the basis of a detailed comparison we also selected it as the oscillator circuit for a cognitive radio spectrum sensor unit [7.39]. Therefore, it is a valid reference circuit for large tuning-range oscillators. The designing of such an oscillator for 0.13-μm CMOS technology is repeated here. The circuit consists of two single-ended three-stage current-starved inverter chains. Small cross-coupled inverters couple these chains. Inverters have the basic structure consisting only of a PMOSFET and NMOSFET devices. The supply for the

inverter chains is delivered from a current mirror that is used to tune the circuit. Table 7.5 summarizes the simulated performance.

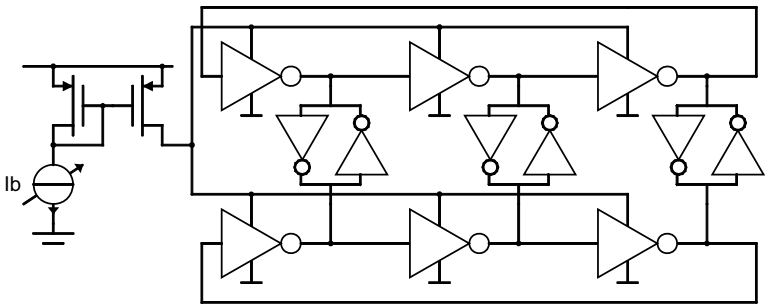


Figure 7.12. Three-stage pseudo-differential ring oscillator.

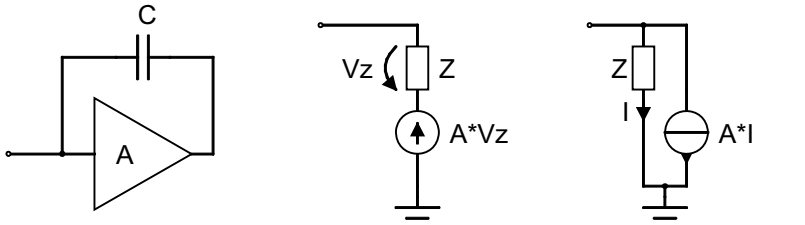
Table 7.5. Performance summary for the ring oscillator.

Frequency range	1.3 – 4.3 GHz
Current consumption	2.8 – 10.7 mA
Phase noise @ 1 MHz	-84 – -86 dBc/Hz

First observation is that all these circuits have a high phase noise level. Actually, in real implementation they would do even worse, because tuning with a current source will inject some additional noise and disturbances. We observe that the active inductor oscillators are noisier and have a narrower tuning range than the described ring oscillator. A simple explanation for the higher phase noise in AIOs is the low oscillation amplitude. In AIOs the signal headroom is quite limited, and previous examples had an oscillation amplitude of only about 100…200 mV_{pp}, while ring oscillators have a rail-to-rail signal.

7.3 Active Tunable Capacitors

Miller capacitance is a well-known nuisance in amplifier design. Effectively, the parasitic feedback capacitance is multiplied by the gain of the amplifier. Generally, this is an unwanted feature, but it can be exploited as well. In a wider scope the Miller effect is a manifestation of impedance multiplication. In such circuits the voltage or current of a passive element is sensed and multiplied with an appropriate device. For the sake of convenience, Figure 7.13 depicts the Miller capacitor, series-mode impedance multiplier, and parallel-mode impedance multiplier. This section deals with capacitors which exploit active circuitry for capacitance tuning. The first subsection describes the principle of capacitance multiplication – the Miller capacitor – and then the second subsection is on the variable impedance converter principle – current steering with the Gilbert cell. The third subsection presents a set of oscillators based on these circuit techniques implemented in a 0.8-μm BiCMOS technology. These circuits were presented in [7.40]-[7.43], and the comparison to alternative passive capacitors was presented in [7.44].



$C_{in} = C(1-A)$ $\quad Z_{in} = Z(1+A)$ $\quad Z_{in} = Z/(1+A)$

Figure 7.13. From the left, the Miller capacitor, series-mode impedance multiplier, and parallel-mode impedance multiplier.

7.3.1 Miller Capacitor

The idea of Miller capacitance is presented on the left in Figure 7.13. A voltage amplifier with a capacitive feedback has an effective input capacitance C_{eff}, which can be either positive and larger than the feedback capacitor C, or negative depending on the voltage-gain A of the amplifier. Both cases can be used in several applications. Here we concentrate on generating a tunable positive capacitance, i.e. the amplifier is an inverting one with A<-1. In a practical amplifier circuit, especially in the GHz-range, there are many non-idealities. The amplifier has a finite input impedance Z_{in}, a voltage gain A, a signal phase shift ϕ, and a finite output impedance Z_{out}. In our target applications the capacitor will be used in a one-port arrangement, meaning that the opposite node is at signal ground. The input capacitance can therefore be embedded into C_{eff}, and any feedback capacitance over the amplifier can be included into the actual feedback capacitor C. Therefore, a realistic, yet sufficiently simple model is to approximate that the amplifier is unilateral and has purely real input and output impedances.

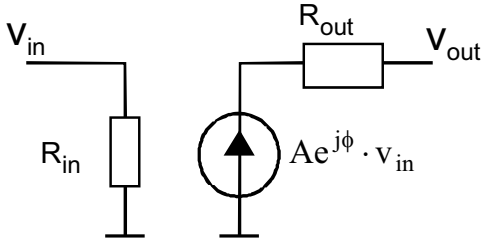


Figure 7.14. Simple analytical model of the voltage amplifier.

The input admittance Y_{in} of a Miller capacitor can be expressed as

$$Y_{in} = \frac{1}{R_{in}} + \frac{\left(1 - A\cos\phi\right)\omega^2 C^2 R_{out} + \omega CA\sin\phi}{1 + \omega^2 C^2 R_{out}^2} + j\frac{\left(1 - A\cos\phi\right)\omega C - \omega^2 C^2 R_{out} A\sin\phi}{1 + \omega^2 C^2 R_{out}^2} \tag{7.13}$$

and the effective capacitance can be formulated as

$$C_{eff} = \frac{(1 - A\cos\phi)C - \omega C^2 R_{out} A\sin\phi}{1 + \omega^2 C^2 R_{out}^2} \tag{7.14}$$

If R_{out}=0 and ϕ=0, then Equation 7.14 is reduced to the basic definition of Miller capacitance. Furthermore, Equation 7.13 indicates that a high R_{in} is required for a high Q-value. Thus, good operation requires high input impedance and low output impedance – the common requirements for a voltage amplifier. To be able to study the effects of other parameters in a simple form, we will ignore R_{in} in Equation 7.13 for a while. Then the Q-value can be expressed as

$$Q = \frac{\left|\,\mathrm{Im}\{Y_{in}\}\,\right|}{\mathrm{Re}\{Y_{in}\}} = \frac{1 - A\cos\phi - \omega CR_{out} A\sin\phi}{A\sin\phi + (1 - A\cos\phi)\omega CR_{out}} \tag{7.15}$$

These equations can now be used for studying the properties of the Miller capacitance circuit. Figure 7.15 shows the effective capacitance and the corresponding Q-value simulation results with three gain settings and two output resistance values. The figures reveal that even in the presence of moderate output impedance high-Q operation can be achieved. Only the required phase shift for the high-Q mode is shifted. This analysis indicates that an amplifier with high input impedance and low output impedance is needed, and by designing it to have the proper phase shift we may achieve a high-Q artificial capacitor. At high frequencies these requirements mean that we need a multi-stage amplifier.

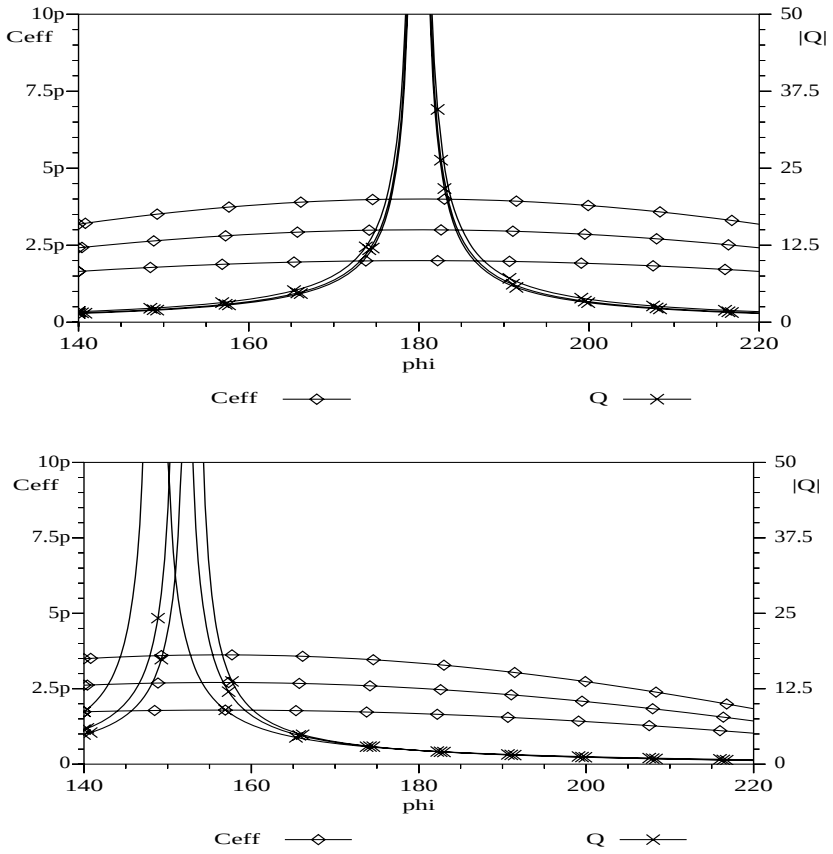


Figure 7.15. Effective capacitance and corresponding Q-value plotted as functions of phase shift ϕ with three values (A=3,5,7) for the gain A. The feedback capacitance is 0.5 pF and the frequency is 2 GHz. In the upper picture R_{out}=0, and in the lower one R_{out}=70 Ω.

7.3.2 Current Steering

The well-known Gilbert cell, often used as an analog multiplier or a variable-gain amplifier, can be used for current steering. Chen and Wu have introduced this idea for capacitance tuning [7.45]-[7.47]. The principle is that the signal current flowing through a floating capacitor is tuned with the current steering circuit. The schematic of such a circuit is shown in Figure 7.16. It is a balanced circuit and in the following analysis the left half-plane is studied. First, let us assume that the transistor Q3p is an ideal transconductor. In that case we can write

$$\frac{v_{in+}}{i_{c+}} = \frac{1}{g_m} + \frac{1}{j\omega 2C} \tag{7.16}$$

Now, if we assume that all of the signal current i_{in+} flows through Q1p, we have capacitive input impedance with a series resistance. With the transistor pairs Q1 and Q2 we can now change the amount of signal current, which flows through the capacitor. If Q1p and Q1m are on and Q2p and Q2m are off, the input is equal to C. In the extreme opposite case the current flows in the reverse direction and the input capacitance is -C. When both pairs Q1 and Q2 are on and in balance, no signal current flows through the capacitor. In this case the input capacitance is equal to the parasitics of the transistors. As the steering circuit is analog, we have a tunable capacitor which varies from -C to C. A more sophisticated and profound analysis of this subject is given in [7.47].

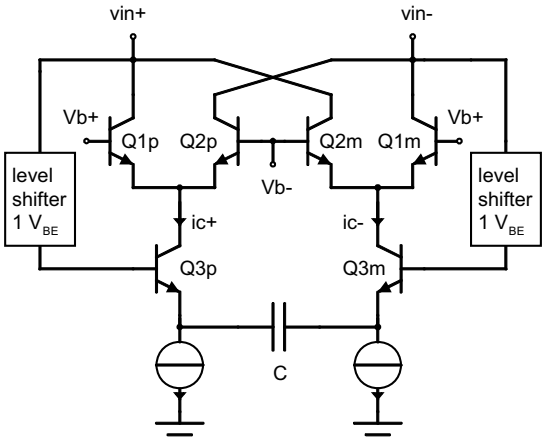


Figure 7.16. Tunable capacitor based on current steering.

7.3.3 Oscillator Implementations

On the basis of the previous ideas, a high-Q Miller capacitor oscillator was first designed and measured. Thereafter, a set of six low-Q Miller-capacitor oscillators were designed (*MillerVCO1*…*MillerVCO6*). Furthermore, two current steering capacitor oscillators (*VICO1* and *VICO2*) were implemented. The circuits were fabricated in a double-metal double-poly 0.8-µm BiCMOS process. The *VTTB8* process has bipolar transistors with 16 GHz cut-off frequencies. Some further details and discussion of the shortcomings of this process will appear in Section 9.2. Regarding the design procedure, although the designs of these circuits were performed using a state-of-the-art of its time RF circuit simulator (*HP MDS*), it had severe convergence problems and the phase noise simulations failed altogether.

High-Q Miller Capacitor Oscillator

In the previous analysis of the Miller capacitance it was observed that the Q-peaking is shifted with the gain and output impedance of the amplifier. Lacking very low output impedance at high frequencies, the required amplifier will consist of at least two inverters and a phase shifter. The aim here was to design the VCO in such a way that the Miller capacitance operates in the high-Q region during tuning. There are several approaches available for the gain tuning. The load can be altered, or we can tune the feedback of the amplifier. In [7.48], the supply voltage was used to tune the Miller capacitance of an amplifier. The drawback of this method is the large on-chip capacitors that are required. Finally, maybe the simplest method is to tune the bias current of the amplifier. With the requirements of high input impedance and low output impedance being kept in mind, the circuit shown in Figure 7.17 was developed. The amplifier includes two inverters (Q2, Q3) with a common RC-series feedback. The current of these inverters is tuned with a simple current mirror (Q5-Q6). The input stage (Q1) has to be of the common-collector type because the input is only connected to the supply voltage through an inductor as shown in Figure 7.18. Finally, the output stage (Q4) also has a common-collector configuration to provide a low output impedance. This artificial varactor has a capacitive tuning range of roughly 8:1 and the corresponding Q-values are over twenty. A simple cross-coupled pair oscillator was built around these capacitors as shown in Figure 7.18. The oscillator includes 3.9-nH single-ended coils designed and modeled by the author. A two-stage common-collector output buffer provides a high input impedance and good output matching to the 50-Ω measurement environment. The measured oscillation frequency and the corresponding phase noise versus the tuning voltage are shown in Figure 7.19. The linear tuning range of almost 400 MHz (17%) is a promising result, but Figure 7.19 also depicts how

the phase noise is really high in the high-Q region near the tuning voltage of 1.8 V. In the high-Q region the Miller capacitance generates excess noise, thus contaminating the oscillator phase noise characteristics. In addition, the frequency range that was measured was higher than the simulated one. In this circuit the oscillation amplitude is limited by the non-linearity of the amplifier of the Miller capacitor. It seems that the gain is even smaller than in simulations, thus leading to a smaller capacitance, and thus a higher oscillation frequency.

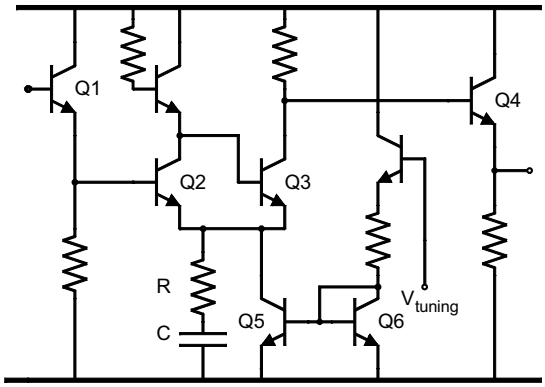


Figure 7.17. Amplifier for high-Q Miller capacitor.

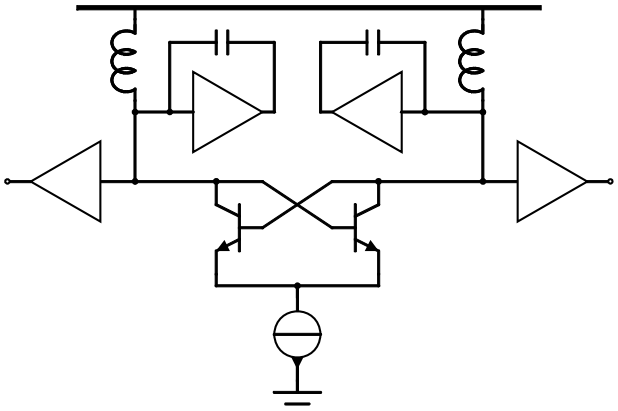


Figure 7.18. Balanced oscillator with high-Q Miller capacitors.

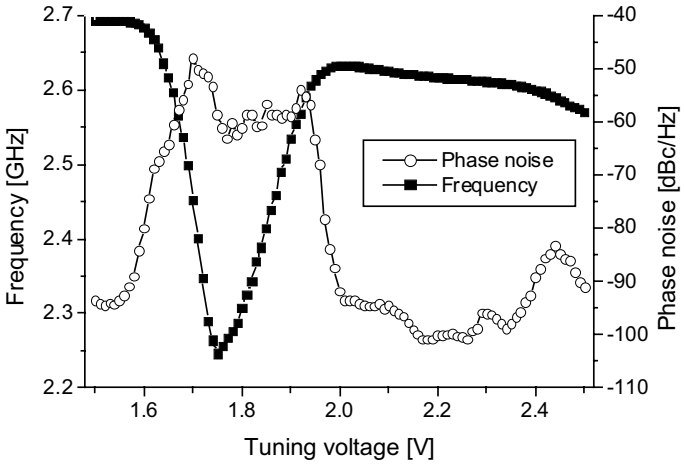


Figure 7.19. Measured oscillation frequency and phase noise at 1-MHz offset for high-Q Miller oscillator.

Low-Q Miller Capacitor Oscillators

Although the results from the previously described circuit are poor in themselves, they were valuable in the sense that they gave us guidelines for the future work. First of all, since the resonator quality factor is dominated by the low-Q component ($Q_{res}^{-1} = Q_{ind}^{-1} + Q_{cap}^{-1}$), it is not worth targeting a really high-Q capacitor, as the inductor Q-value is as low as three. Hence, it is sufficient to have a Q-value around ten for the Miller capacitor and even with a value equal to the Q-value of the inductor, the total Q-value is only reduced by a factor of two. The lower Q-value of the Miller capacitor will reduce the noise significantly compared to the previous high-Q case. Second, in Section 7.3.1 we found out that the Q-value of the Miller capacitor is associated with the phase shift of the amplifier. Thus, it would be desirable to have a constant phase shift regardless of the operating frequency or the gain of the amplifier. Then the Q-value would not change when the oscillator is tuned. This cannot be achieved totally, but it is worth keeping in mind during the actual circuit design. Third, the value of the Miller capacitance depends on the oscillation swing because the swing is limited by the nonlinearities of the amplifier, i.e., the amplifier operates in the compressed mode. Thus, the operating frequency and the output power depend on the nonlinear characteristics of the amplifier in the Miller capacitor. This type of situation is extremely sensitive to the accuracy of the device models, simulator characteristics, and process spread. This problem can be circumvented either by designing a sophisticated amplifier with well-predictable and stable compressed mode operation or by limiting the oscillation amplitude with the negative conductance circuit in such a way that the Miller capacitor operates in the linear region. Finally, in the high-Q VCO both Miller capacitors had an amplifier of their own. These should be combined into an appropriate differential amplifier circuit. This would lead to lower power consumption, save die area and improve linearity because even harmonics are suppressed.

Six circuits were designed. The circuit diagrams of the VCOs are depicted in Figure 7.20. These include four different types of amplifiers and two types of negative-conductance circuits. In the first circuit, *MillerVCO1*, the amplifier, depicted in Figure 7.21a, consists of a common-emitter (CE) Darlington stage followed by a common-collector (CC) output stage. The negative conductance is generated with a simple cross-coupled transistor pair. In this circuit the amplifier for the Miller capacitor tolerates a DC input level equal to the supply voltage. Thus, the inductors are connected directly to the supply node. In the rest of the circuits the amplifier has to have a lower DC input level. In these circuits the inductor is floating and the supply is fed through a high-impedance load (V_{BE}-multiplier), which sets the appropriate DC levels. In *MillerVCO2* the amplifier, depicted in Figure 7.21b, consists of a CE-stage, again followed by a CC-stage. In *MillerVCO3* the signal path includes a combination of CE-CC stages and CC-CB stages, as shown in Figure 7.21c. *MillerVCO4* is similar to *MillerVCO3*, with the exception that the bases of the CB-transistors are connected to the opposite input nodes, as depicted in figure 7.21d. MillerVCO1-4 use a conventional CCP structure, while *MillerVCO5* and *MillerVCO6* have similar Miller capacitors to *MillerVCO1* and *MillerVCO2*, but in these circuits the negative conductance is generated with a cascode CCP-structure that will be described in Section 9.2. This CCP structure has high negative conductance and small input capacitance. However, it suffers from a low signal swing capability. We are using it here to limit the oscillation swing and thus enable the amplifier of the Miller-capacitor to operate in the linear region.

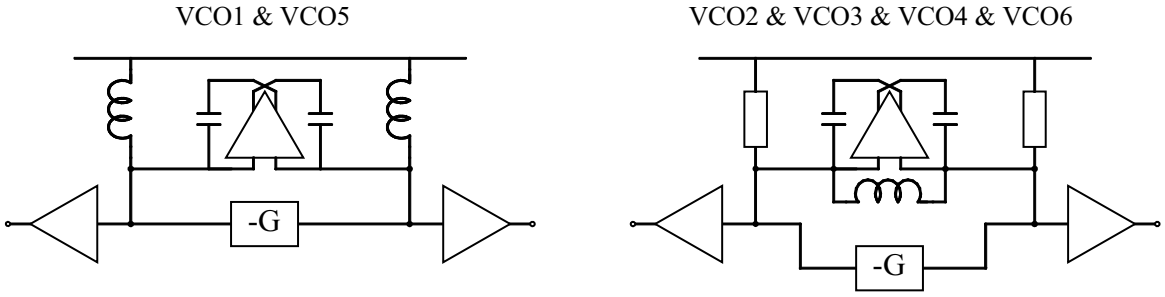


Figure 7.20. Simplified schematics of low-Q Miller VCOs.

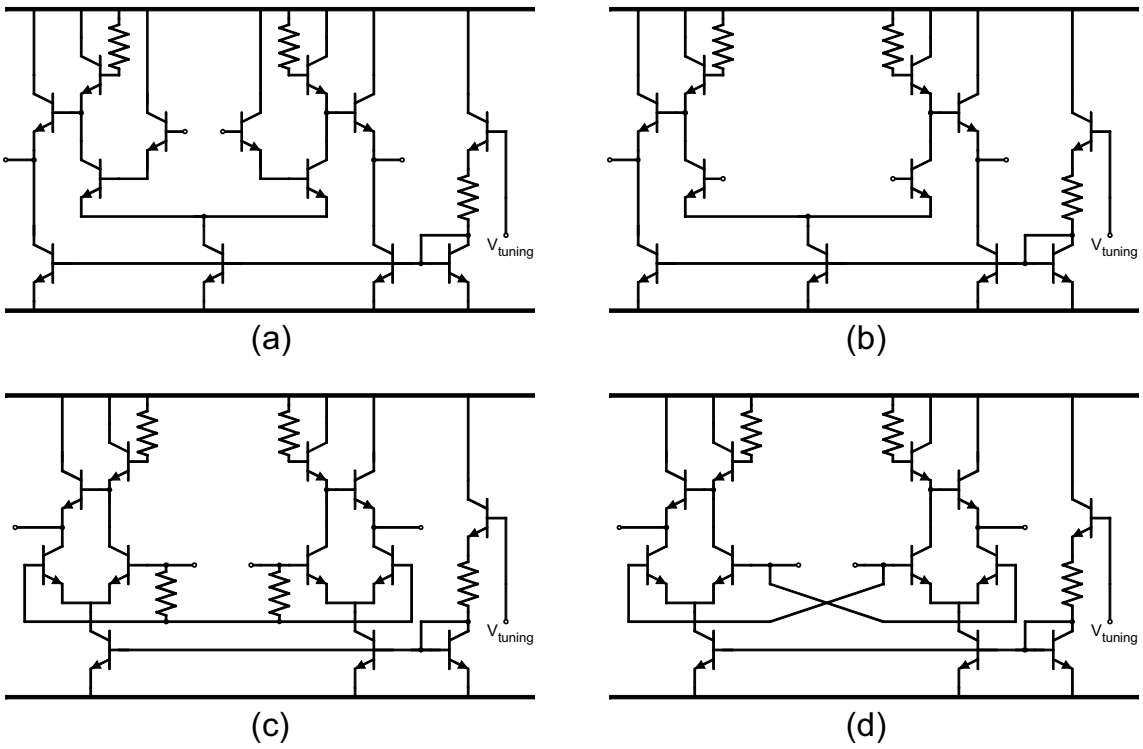


Figure 7.21. Amplifiers used for creating the Miller effect. (a) The circuit used in *Miller*$_{VCO1}$ and *Miller*$_{VCO5}$. (b) The circuit used in *Miller*$_{VCO2}$ and *Miller*$_{VCO6}$. (c) The circuit used in *Miller*$_{VCO3}$. (d) The circuit used in *Miller*$_{VCO4}$.

Current Steering Oscillators

Figure 7.22 shows a variable impedance converter oscillator, *VICO1*. It includes the basic Gilbert cell configuration for capacitance tuning. In this circuit the negative conductance is generated with a transistor pair including emitter degeneration. The usefulness of this structure relies on the fact that now the negative conductance circuit also acts as a level shifter, and therefore no actual level shifters are needed in the current steering circuit. On the other hand, emitter degeneration reduces the amount of negative conductance that is generated, $g_{in} = -g_m /(1+\frac{1}{2} g_m R_E)$. To avoid this loss, the second circuit, *VICO2*, includes a cross-coupled transistor pair with level shifters. *VICO2* is similar to *VICO1*, with the only difference being in the structure of the negative conductance circuit. The circuit is depicted in Figure 7.23.

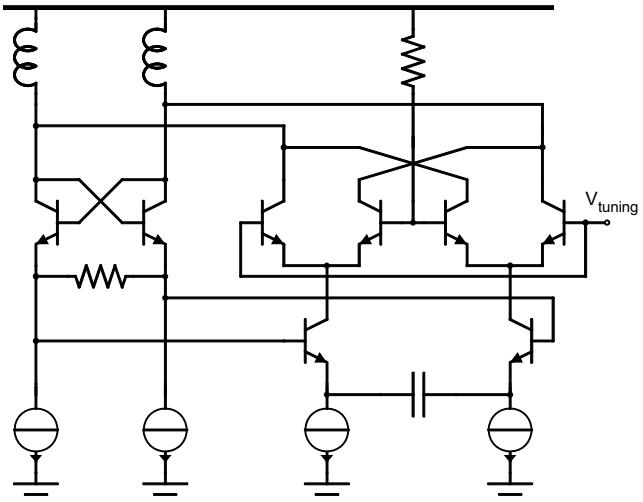


Figure 7.22. Variable impedance converter oscillator *VICO1* (buffers are omitted).

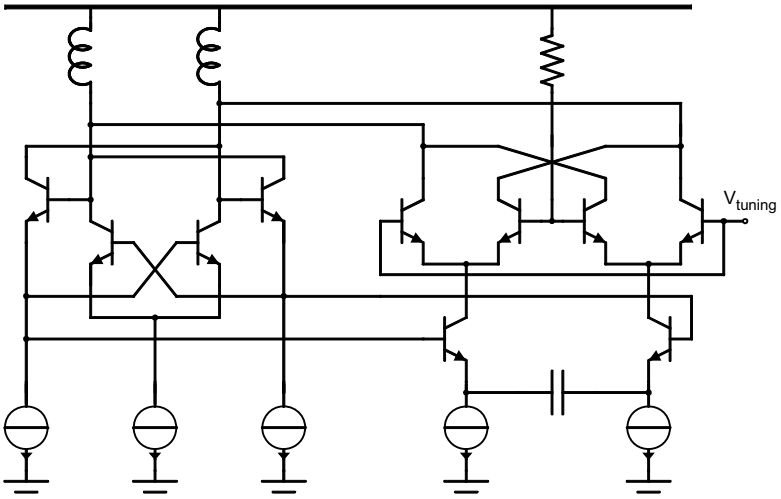


Figure 7.23. Variable impedance converter oscillator *VICO2*. (buffers are omitted).

Results

Figure 7.24 depicts a 5-mm^2 die that includes the six MillerVCOs, two VICOs, three inductors, and a pn-junction diode test structure. Figure 7.25 shows a closer view of *MillerVCO2*. The size of the circuit, including the pads, is 730x680 μm^2. The simulation and measurement results are compared in Table 7.6. In the simulations all the circuits have a wide tuning range, flat output power, and reasonable power consumption. The VICOs have higher oscillation frequencies because they partly compensate for the parasitic capacitances of the monolithic inductors and negative-conductance circuits. Several samples were measured on-wafer and only a fairly small deviation was noticed. For the following results a typical sample of each circuit was selected. All the circuits oscillated, but *MillerVCO5* and *MillerVCO6* did so with a low output power. The best Miller capacitor VCOs seem to be *MillerVCO1* and *MillerVCO4*. For these the tuning curve and corresponding phase noise are shown in Figures 7.26 and 7.27. Similar measurement results for *VICO1* and *VICO2* are depicted in Figures 7.28 and 7.29. In the phase noise curves one may observe clear dependency between the VCO gain and phase noise. *MillerVCO1* is better than *MillerVCO4* but has clearly smaller tuning range as well. In *VICO*-circuits phase noise is almost flat at region of the almost-constant VCO gain. One may consider finding a slight maximum at region where the transition from –C to +C takes place. *MillerVCO4* presents something we were looking for: a wide tuning range and reasonable

power consumption. However, in *MillerVCO4* we still have a peak in the phase noise curve. This is partly explained by the higher VCO tuning gain, and by the corresponding higher sensitivity to both internal and external noise sources. With improved circuit structures a slight improvement might be possible, and yet the noise would still be high. Both VICOs have wide tuning ranges with fairly good tuning linearity, but the phase noise is high in *VICO2*. The only difference between *VICO1* and *VICO2* was in the structure of the negative resistance circuit. Consequently, the additional phase shift caused by the voltage followers causes the phase noise to deteriorate. If the tunable capacitor in *VICO2* is simulated alone, it appears that the input impedance has a negative real part as a result of this phase shift. Hence, the existence of two negative resistances seems to cause poor phase noise. By comparing our *VICO1* with the one published in [7.47], we can notice that the results are quite equal. Our circuit has a tuning range of 42 % while in [7.47] it is 30 %. They report a phase noise of –86 dBc/Hz at a 100 kHz offset, which can be estimated to be equal to -106 at a 1-MHz offset. This value was measured at the end of the tuning curve. From the same point we measured -110 dBc/Hz. In [7.47] the power consumption is lower, 30 mW vs. our 51 mW. Finally, if we compare Miller capacitor oscillators to these VICOs, the main message is that Miller capacitor VCOs are more difficult to design and they are more sensitive to all kinds of errors, such as device model inaccuracies or process spread. It is hard to see any particular reason to favor them.

Table 7.6. Comparison of the simulation and measurement results of the oscillators.

Circuit	Simulations			Measurements			
	f_{center} [MHz]	Tuning range	P_{DC} [mW]	f_{center} [MHz]	Tuning range	$\mathcal{L}$(1MHz)* [dBc/Hz]	P_{DC} [mW]
High-Q VCO	1925	23 %	66	2470	18 %	-50	60
MillerVCO1	2080	21 %	45	1590	15 %	-80	36
MillerVCO2	2080	18 %	54	1840	29 %	-70	39
MillerVCO3	2000	15 %	36	2100	12 %	-70	25
MillerVCO4	1960	24 %	42	1820	30 %	-70	26
MillerVCO5	2350	21 %	57	2480	22 %	-50	18
MillerVCO6	2370	23 %	54	2240	46 %	-60	31
VICO1	2780	23 %	42	2570	42 %	-90	51
VICO2	2880	19 %	42	2180	29 %	-70	51

* Rounded worst value within the tuning range.

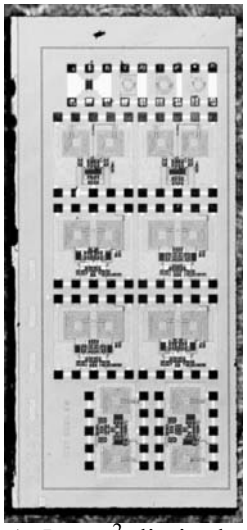


Figure 7.24. A 5-mm^2 die including six MillerVCOs, two VICOs, three inductors, and a pn-junction diode test structure.

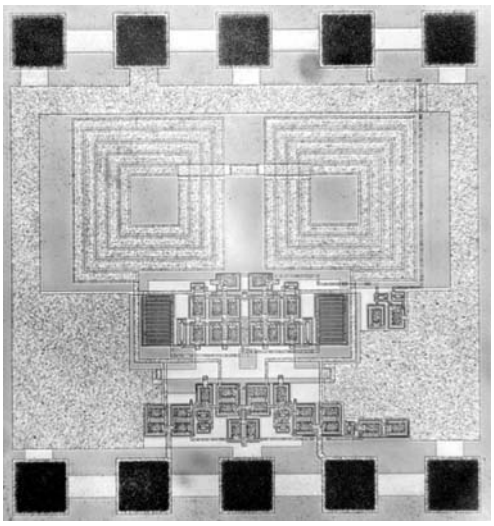


Figure 7.25. Microphotograph of *MillerVCO2*.

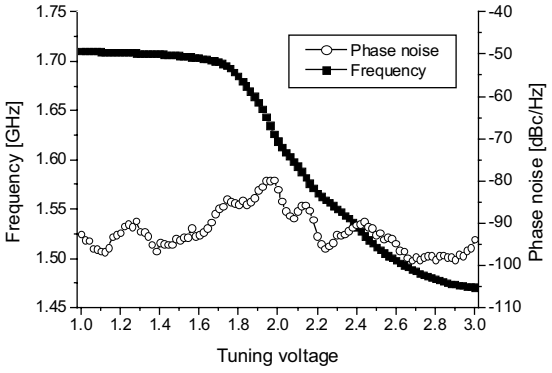


Figure 7.26. Measured oscillation frequency and corresponding phase noise at 1-MHz offset from the carrier for *MillerVCO1*.

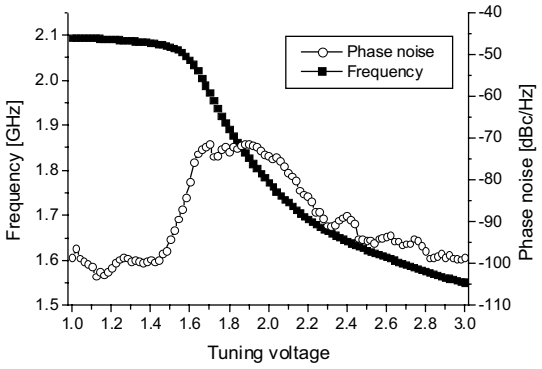


Figure 7.27. Measured oscillation frequency and corresponding phase noise at 1-MHz offset from the carrier for *MillerVCO4*.

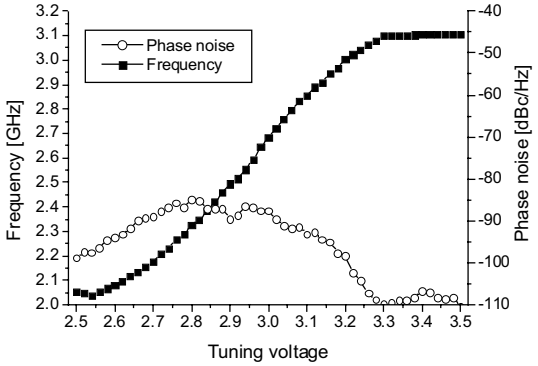


Figure 7.28. Measured oscillation frequency and corresponding phase noise at 1-MHz offset from the carrier for *VICO1*.

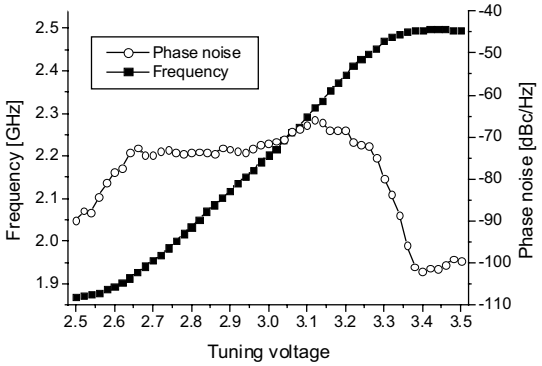


Figure 7.29. Measured oscillation frequency and corresponding phase noise at 1-MHz offset from the carrier for *VICO2*.

7.4 Conclusions

Artificial reactive elements can be used in RF oscillators. They do offer a wide tuning range, but suffer from high noise. Although in small-signal analysis these elements may show high Q-values, this is not a correct design choice. Instead, a lower oscillator phase noise is observed in low-Q active reactive circuits. Furthermore, oscillators based on active tuning elements have small signal-headroom within the active circuit and their characteristics vary with frequency. Frequency dispersion and signal-level dependent reactance cause design difficulties, high sensitivity to device parameter spread, and poor predictability with real-life non-ideal device models.

A simple useful way of thinking is to consider that noise causes the actual reactance value to fluctuate in artificial reactive elements. Therefore, oscillators based on these elements have high phase noise, and they rarely if ever show a better performance than more commonly used oscillators, such as ring oscillators. It is hard to see any use for these circuits, not at any rate in the context of RF oscillators.

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8 Quadrature Signal Generation and Frequency Conversion Circuits

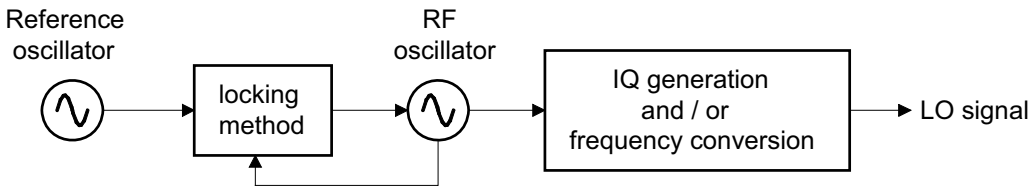


Figure 8.1. General scheme for LO signal generation.

Figure 8.1 depicts a general arrangement for LO signal generation. Indirect frequency synthesis techniques apply a locking method to couple the RF oscillator to a clean low-frequency source. Phase locking is the prevailing technique, but injection locking, delay locking, or even pure frequency locking may be applicable as well. Most modern radio systems utilize such an architecture that the in-phase (I) and quadrature-phase (Q) LO signals are needed. Therefore, this IQ signal generation is an axiomatic part of the LO frequency synthesis. Techniques for IQ signal generation are studied in Section 8.1. Three common circuit techniques are discussed in the three subsections. Passive RC phase shifters, and particularly polyphase RC filters, are studied first. Then IQ generation with a divide-by-two frequency divider is considered. The third alternative is coupled oscillators. Section 8.2 deals with frequency conversion techniques. These are used to enhance the number of frequency bands that are generated, or to alleviate some coupling problems. Two detailed case studies are included in this chapter to demonstrate these frequency converters in a slightly more practical level. Section 8.3 presents a frequency synthesizer based on a single sideband mixing method for ultra-wideband radios, and Section 8.4 presents a frequency conversion unit for a direct period synthesizer.

8.1 Quadrature Signal Generation

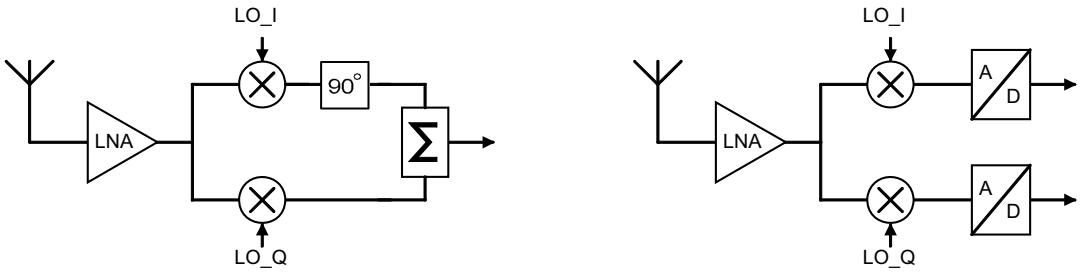


Figure 8.2. On the left, an image-reject Hartley receiver, and on the right a direct-conversion receiver.

Figure 8.2 depicts two commonly-used receiver architectures. In the Hartley receiver [8.1], image frequency rejection is achieved by using complex mixing. It can be shown [8.2],[8.3] that in an ideal case without imperfections the image frequency is rejected. In practice, the phase deviation $\Delta\theta$ and amplitude ratio A_{bal} of the two signal-paths result in a finite image-rejection ratio (IRR) given by [8.2],[8.3]

$$IRR = \frac{1 + 2A_{bal}\cos\Delta\theta + A_{bal}^2}{1 - 2A_{bal}\cos\Delta\theta + A_{bal}^2} \tag{8.1}$$

The phase and amplitude mismatches cumulate throughout the complete signal paths. So, instead of just the LO imbalance, the single-to-differential conversion near the input, mixers, and the low-frequency phase shifter and summing circuit also contribute to the overall image rejection. In the RC circuits described later there is error only in phasing or in amplitude, and therefore it is convenient to simplify Equation 8.1 with cases that have only phase error or amplitude imbalance. These two results also imply that we can use the IRR value as a general figure of merit for the IQ balance.

$A_{bal}=1$ $$IRR_{phase} = \frac{1+\cos\Delta\theta}{1-\cos\Delta\theta} \tag{8.2}$$

$\Delta\theta=0$ $$IRR_{ampl} = \left(\frac{A_{bal}+1}{A_{bal}-1}\right)^2 \tag{8.3}$$

The two sidebands of the RF carrier contain different information in communication systems utilizing phase- or frequency modulation methods. Therefore, it is necessary to generate separate I and Q channels in direct-conversion receivers (DCR) to avoid the overlapping of the sidebands when they are down-converted around DC. An IQ imbalance degrades the signal-to-noise ratio (SNR) of the receiver. Actually, in DCRs phase imbalance is more serious than amplitude error [8.4]. A phase error of one degree causes practically negligible deterioration of the performance [8.5], and for typical DCRs for 2G/3G communication systems an IQ balance of just about 25 dB is sufficient [8.5]. In modern OFDM modulation IQ inaccuracy causes some of the power in the -nth subcarrier to fold on top of the +nth subcarrier, which eventually leads to a worse SNR [8.6]. For instance, one WLAN system simulation showed IRR requirement of 40 dB [8.7]. With the common RF circuit techniques 30 – 40 dB image rejection can be achieved. With automatic post-tuning, and/or with further baseband digital signal processing [8.8],[8.9] IQ imbalance compensation can be performed. To sum up, the exact requirement for the IQ balance of an LO signal depends on the receiver architecture, on the modulation method applied, and on the performance of the DSP unit.

8.1.1 RC Phase Shifters

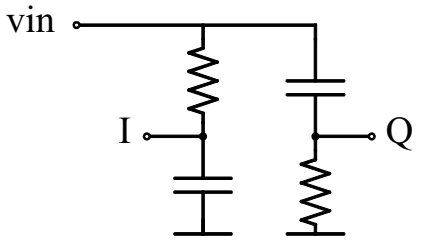


Figure 8.3. RC-CR network with constant IQ phase balance

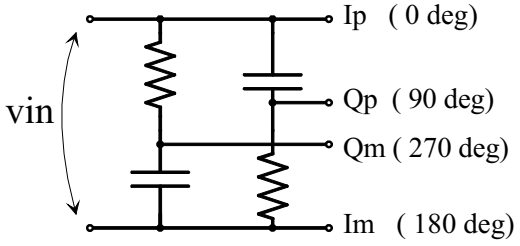


Figure 8.4. RC-CR network with constant IQ amplitude balance

The simplest way of generating the IQ signals is with an RC-CR network, as shown in Figure 8.3. At the pole frequency $1/(2\pi RC)$ the signal at the I-output has a 45-degree phase lag, and the the signal at the Q-output has a 45-degree phase lead. Both signals have been attenuated by 3 dB. So, at the pole frequency both phase and amplitude are in balance. This structure offers a constant 90-degree phase shift over all frequencies but suffers from amplitude imbalance. A remedy is to add clipping amplifiers after the RC-CR network [8.10]. If the signal is amplified up to rail-to-rail the amplitude error vanishes, and theoretically we have an excellent IQ signal. This approach has a drawback, though. If the input signal is asymmetric, i.e. a distorted sinusoid or a square wave with a non-50 % duty cycle, the IQ signal will have a phase error. In

addition, square wave type LO signals are desired in some applications, while in others the LO signal needs to be sinusoidal. In these cases hard mixing that generates mixing products at odd harmonics is not acceptable. Yet another problem is component mismatch. It results in the two RC products being unequal, and this generates a phase error. In modern technologies with skillful layout design, a mismatch of roughly 1% can be achieved, and this results in a good quadrature accuracy (i.e. IRR) of about 40 dB. As such, device mismatch is inversely proportional to the area that is occupied, and it can also be reduced with the use of dummy devices. Hence, better matching is achieved with a larger die area. R and C process variations obviously shift the pole frequency, and thus a pure RC-CR network without clipping amplifiers is susceptible to process spread. Finally, if we make just a tiny rearrangement and use the RC-CR circuit in a balanced configuration, as shown in Figure 8.4, the network has unity amplitude balance at all frequencies, but now it has phase error [8.11]. Both the differential I and Q signals are themselves in exact balance, but the I/Q paths have phase error. On the basis of the previous discussion, this is not an attractive approach since it is more difficult to compensate phase error than amplitude error. The RC-CR technique became less popular in the late 1990s as a result of emergence of the polyphase filter technique and improved technologies that made low-power divide-by-two circuits feasible. Nevertheless, the method has its benefits, and for instance *Broadcom* utilized it recently [8.12].

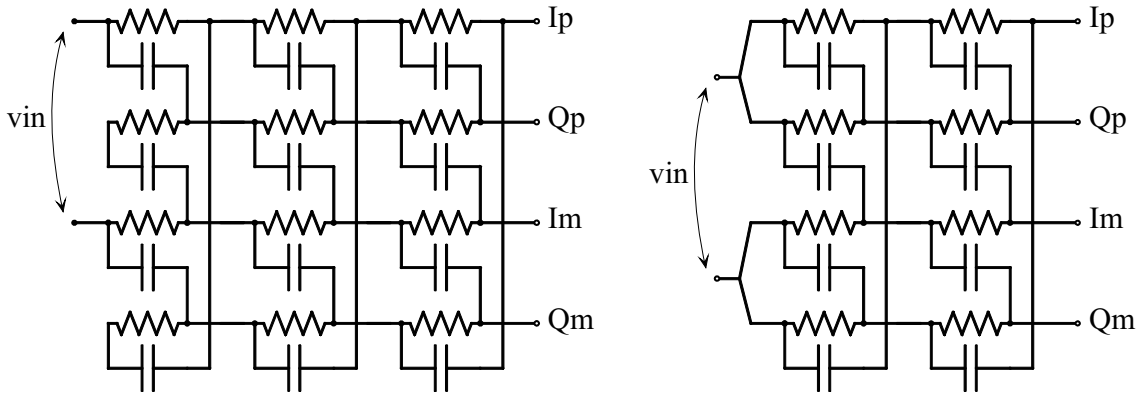


Figure 8.5. Three-stage Type I polyphase filter (PPF) on the left, and on the right two-stage Type II PPF.

Polyphase filtering for quadrature generation was originally proposed by Gingell in 1973 [8.13]. He called them sequence asymmetric polyphase networks, where the term 'asymmetric' refers to the ability of the network to suppress or pass signals according to its phase. In plain words, a polyphase RC filter (PPF), depicted in Figure 8.5, is a symmetric and repetitive version of a simple RC-CR network. In contrast to the previously discussed RC-CR networks, the PPF is less sensitive to absolute variations of C and R. This is easily accomplished by putting into cascade more than one stage, which makes the transfer function of the circuit broadband. This improves the IQ balance. The PPF concept remained less well known within the RF IC community until the mid-1990s. Since then this technique has become widely exploited. Personally, I have studied and used this approach in two projects that will be described in Sections 9.3 and 9.5. During these works we found out that despite their wide popularity, publications on the detailed analysis and explanation of the design principles of RC PPF remained few [8.14],[8.15]. This is easy to understand, since even the basic derivation for the transfer function of just a one-stage PPF is a somewhat tedious task. We tackled the challenge, and published a comprehensive analysis in [8.16]. I do not intend to repeat all that mathematically intensive work here, but just to summarize the main results. In addition to [8.16], some extended material exists in Kaukovuori's dissertation [8.17].

An RC polyphase filter consists of RC stages that can easily be cascaded. Each stage consists of four capacitors and four resistors, as depicted in Figure 8.5. The figure also illustrates the two alternative arrangements for feeding the PPF. With the input arrangement of a Type I PPF, the circuit has only amplitude error, while in a Type-II PPF the IQ imbalance is due to phase error. Figure 8.6 (from [8.18]) depicts a comparison of three PPF cases. A three-stage case with all its RC poles equal is compared to two- and three-stage cases with unequal, i.e. split, RC poles. One may observe that increasing the number of stages results in a higher IRR at a wider bandwidth. It is worth to remember that this wider bandwidth is equal to better tolerance for RC process spread. Decisions on the number of stages, type of input feeding, pole splitting, and absolute values of R and C are the tools of the designer in practical RC PPF dimensioning. The following text briefly gives some basic guidelines for PPF design. Further details and explanations on forthcoming text can be found in [8.16].

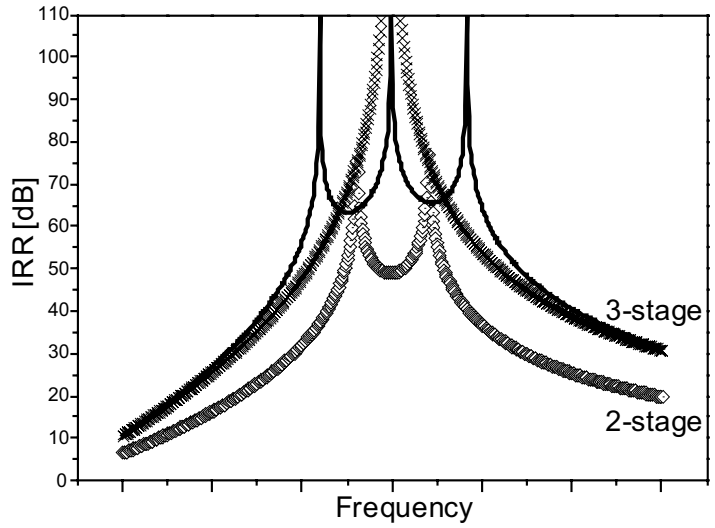


Figure 8.6. Image-rejection ratio offered by two- and three-stage polyphase filter. The continuous line describes the three-stage case where the RC-poles are split, and the line with cross symbols has all the three poles equal.

Type of PPF

Both Type-I and Type-II PPFs have an equal IRR performance and characteristics related to all the issues mentioned below. The choice of the type is thus just based on the requirements of the application system for its phase or amplitude imbalance. If there is no such preference, then the Type I input arrangement is easier to design, and since the floating inputs are at virtual ground there is no requirement for equal loading or parasitic capacitance.

Number of stages

Each RC stage introduces losses of about 3 dB. Therefore, although increasing the number of stages is an easy method for achieving a high IRR over a large bandwidth, one should use as few stages as possible. A bandwidth wherein the required IRR needs to be achieved is defined by $BW_{IRR}=\omega_{max}/\omega_{min}$. For a PPF with n equal RC stages we have a relation

$$IRR = \left(\frac{\sqrt{BW_{IRR}} + 1}{\sqrt{BW_{IRR}} - 1} \right)^{2n} \tag{8.4}$$

RC pole splitting

Pole splitting increases the bandwidth but results in valleys with a lower IRR value. It turns out that pole splitting is always favorable, and particularly effective if just moderate IRR values are

the target. In the optimum case the poles are split in such a way that the lowest IRR values in the valleys are equal to the required IRR at the borders of the desired band. This idea was studied mathematically in [8.16]. A commonly-used three-stage PPF is a good demonstrator here. First, we define the pole-splitting factors k_2 and k_3 relative to the first pole.

$$k_2 = \frac{\omega_1}{\omega_2} \quad \text{and} \quad k_3 = \frac{\omega_1}{\omega_3}, \qquad k_3 > k_2 > 1 \tag{8.5}$$

By requiring both IRR minima in the two valleys to be equal, we gain $k_3 = k_2^2$.
Now we may bound the pole-splitting factor k_2 with the desired IRR and bandwidth.

$$IRR_{\min} = \left(\frac{\sqrt{k_2}+1}{\sqrt{k_2}-1} \right)^3 \left(\frac{k_2 - \sqrt{k_2}+1}{k_2 + \sqrt{k_2}+1} \right) \tag{8.6}$$

$$BW_{IRR} \approx 2k_2^2 - 1.9k_2 + 0.9 \tag{8.7}$$

Unfortunately, the above equations do not have a simpler closed-form solution. These can be studied numerically or by drawing a graph.

Impedance level: choice of R & C values

Until now in this discussion only the value of the RC pole frequency has had any meaning. Thus, one might arbitrarily select any value for e.g. resistors. As proof, in [8.16], pole splitting reduces the overall loss of a PPF. Then the values of each R and C impact on the overall loss, and with proper choice the losses are minimized. This results in a non-obvious deduction that all capacitors should be of equal size, and the pole splitting is done by scaling the resistors. The first rule for the capacitor value selection is that one should select an optimum impedance level for the PPF in order to minimize the overall losses, according to the finite source (Z_S) and load impedances (Z_L) present in any practical implementation. The study of minimal losses in the presence of Z_S and Z_L also results in a guideline that resistor values, i.e. the RC stages, should be placed in such an order that the impedance level increases among the signal path. Actually, this is just the impedance tapering principle, which is well known in RF engineering. Here it is assumed that the PPF is driven from a low-impedance source and the final load is a high-impedance terminal. The second rule for the capacitor value selection is to choose a value that is sufficiently larger than the parasitic capacitance present at each node. Numerical analysis of the impact of the C/C_{par} ratio shows a knee region, after which the impact saturates. Since the physical properties of capacitors and resistors, and hence the related parasitic capacitance, vary in different processes, it is not possible to give any general guidelines here. Some processes even include alternative types of passive devices, such as resistors with different sheet resistances, and the choice impacts on the parasitic capacitance, device mismatch, and absolute process variation. Furthermore, since device mismatch is related to the component area, small devices prone to mismatch should be avoided. This is a true practical issue, particularly at higher frequencies, where absolute device values are low.

As an example of practical work, Figure 8.7 shows a measured result of a three-stage polyphase filter [8.18]. It is used in a Hartley-type receiver, shown in Figure 8.2, as the phase shift and summing circuit. The functionality is inverse to IQ generation, and yet the principle is the same. The receiver achieves an IRR of over 40 dB within the desired 36-44 MHz IF band. Interestingly, although the PPF has three stages, the middle IRR peak and the corresponding clear valleys are missing from the measured results. Numerical simulations show similar behavior when device mismatch is present.

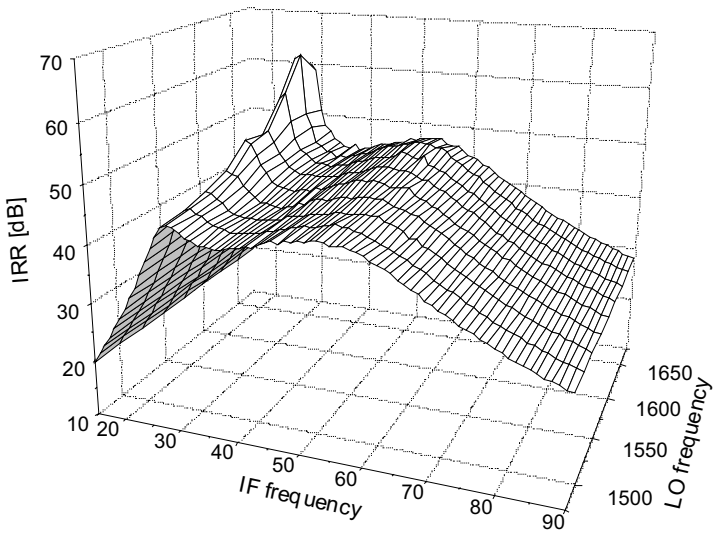


Figure 8.7. Measured image-rejection ratio for a three-stage PPF.

8.1.2 Divide-by-Two Method

A delayed flip-flop (DFF) in a unity feedback arrangement performs a divide-by-two operation. Such a flip-flop consists of two D-latches, as depicted in Figure 8.8. Each latch includes an input tracking stage that, while active, senses the input and sets the output level. The cross-coupled transistor pair stores the signal level while tracking is inactive. Since the output changes its level every second input cycle, the outputs of the two latches are in 90-degree offset at the output frequency. The differential implementation of the latches then provides all the four-quadrant (IQ) outputs. Figure 8.9 (a) depicts the basic source-coupled logic (SCL) latch and one common modification of it. The first modification step to the basic SCL D-latch is to remove the current sink. This allows operation at a lower supply voltage. A circuit with three elements in a stack is able to operate at 1.2-V supply commonly used nowadays. Modifications with only two transistors on top of each other have also been proposed [8.19],[8.20]. In digital-like operating mode the input transistors need to be driven in and out of saturation. This requires a sufficiently large input signal. In such behavior the internal voltage swing is also large and this actually limits the highest toggle frequency. Higher operating frequency with lower power consumption is achieved by avoiding hard switching of the input transistors and by limiting the internal voltage swing in all nodes. Correct operation in all process corners sets a practical limit to the voltage swing level. PMOS loads, biased in the triode region, offer a conveniently low RC time constant at the latch output. Further modification leads to the circuit shown in Figure 8.9b, where the input transistors are AC-coupled and biased to be continuously on. With this minor modification the behavior of the circuit, or the way we consider it, alters significantly. Now the divide-by-two circuit may be interpreted as an injection-locked oscillator (ILO). Without any input signal the circuit oscillates at its natural frequency, and in the presence of a sufficiently strong input signal the oscillation frequency is half of the frequency of the input signal. This way of thinking leads to the use of a sensitivity curve, which is a powerful tool for the proper design of this type of circuit. In the vicinity of the self-oscillation frequency just a small amount of power is needed to pull the frequency, while at larger offsets a larger input signal is also needed. One sensitivity curve is presented in Figure 8.10. The injection locking range is related to the Q-value of the resonator in the oscillator, and to the relative level of the injection signal [8.21]-[8.23]. A DFF-based ILO has a wide locking range since the Q-value is low. If we use coils to boost the operating frequency or to reduce the current consumption, the locking range is reduced.

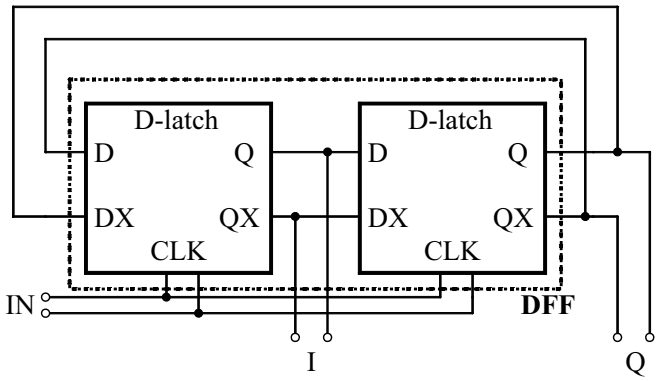
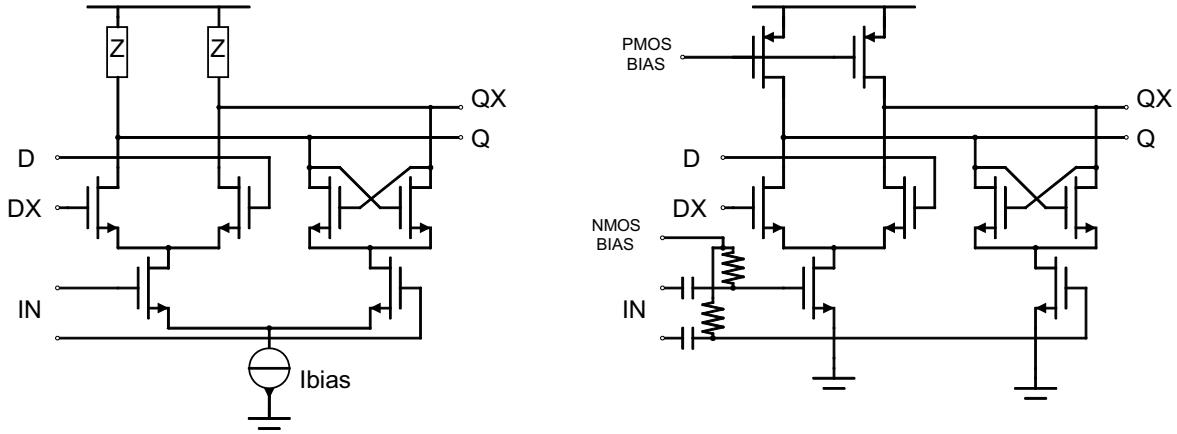


Figure 8.8. The divide-by-two circuit consists of two D-latches, and produces IQ outputs.



(a) (b)

Figure 8.9. (a) Basic SCL latch (b) The same without current source and with AC-coupled inputs and PMOS loads.

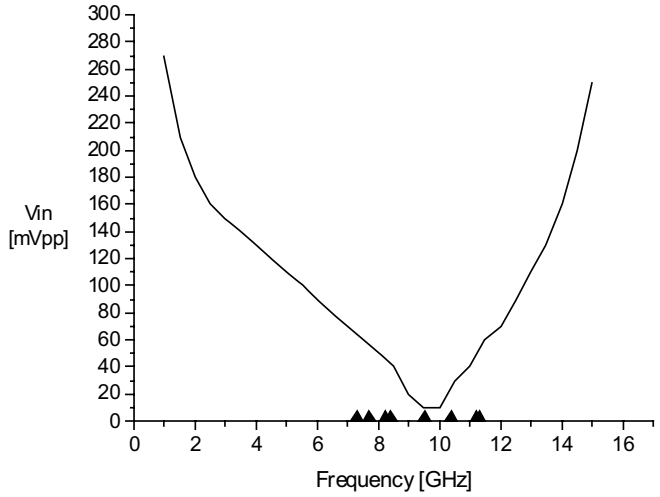


Figure 8.10. Sensitivity curve for a divide-by-two prescaler, designed for a UWB radio LO generator in a 0.13-µm CMOS technology (see Ch. 9.5 for details). The dark triangles represent the self-oscillation frequency at nominal and at various process-spread corners.

There are three sources for amplitude and phase imbalance in divide-by-two IQ generation. Device mismatch and layout asymmetry are quite obvious matters, though challenging to simulate accurately, whereas the impact of the input signal needs attention. The divide-by-two method requires perfectly symmetric input signals for the two latches. Either digital-like square-waves with a 50-% duty cycle or sinusoidal signals with no amplitude or phase error are needed. In practice, producing such signals is difficult and the lack of a good-quality input signal is often the major cause of poor IQ balance. Some simulation results on this issue will be discussed a little later. A rule of thumb is that without specific tuning, such as in [8.24], a DFF-based IQ generator is able to provide just about 20 – 30 dB IRR. Since a divider can reduce the phase and amplitude errors, a common technique to improve the quality of the input signal is to have yet another divider in front of the actual IQ generator. We have also used this approach in our cable-modem project; see Ch. 9.3. Alternatively, one may use a chain of frequency multiplier – frequency divider [8.25],[8.26]. In a laboratory, when measuring prototype front-end circuits, it also important to keep in mind the fact that external phase shifters, which are used for single-to-differential transformation, suffer from both amplitude and phase imbalance.

In RF CMOS frequency dividers, and particularly in IQ generation, derivatives of SCL circuits are used almost exclusively. Other digital circuit families, such as true-single-phase clocked logic (TSPC) [8.27], can also be used. These circuits are single-ended in nature. Although it is possible to create pseudo-differential versions, they are inherently prone to small phase offsets, and thus are not attractive for IQ generation. A potential application is low-power circuits with an operating frequency that is moderate compared to the limits of the technology. Yet another frequency division technique is a regenerative divider, or Miller divider [8.28] as it is often called. These circuits include a mixer, a low-pass filter and an amplifier in feedback loop. Miller dividers are usually used at very high frequencies, where static dividers fail. See e.g. [8.29]. A nice design example of IQ generation with a regenerative circuit is given in [8.26].

Finally, a practical IQ generation circuit is presented. I designed it for a spectrum sensor unit for cognitive radio applications [8.30]. The circuit was designed in a 65-nm CMOS technology, and it is targeted to provide IQ signals for the LTE bands at 0.7-2.6 GHz. Figure 8.11 shows the schematic of the circuit. The circuit includes two D-latches, and simple inverters are able to drive the passive mixer core with almost rail-to-rail signals. The inverters are AC-coupled and include resistive feedback for self-biasing. All the four inverters share the same PMOS switch for power control. According to simulations without layout parasitics, the IQ-generator operates at the input frequency range of 0.2 – 13 GHz with an input signal level of 0.4 V_{pp}, while consuming about 1.5 mA of current. Here we use this design case to analyze the impact of the input signal. This circuit shows an almost linear 5:1 relationship between the input phase error and the IQ phase imbalance up to over 20-degree phase error at the input. In other words, if the sinusoidal input signals are both 0.4 V_{pp}, but instead of having an exact 180-degree phase shift they have a 185-degree phase shift, then at the output the IQ phase error is one degree. The impact of the amplitude imbalance is a somewhat more intricate issue, since it depends on the actual level of the input signals. With moderate input signal levels, the amplitude imbalance at the input converts to phase imbalance at the output, and this relationship is almost linear for small differences. The amplitude imbalance at the output is weak. Here, a ten-degree phase error at the input produces an amplitude imbalance of just 0.2 dB at the output, while with a 100-mV amplitude error in the nominal 0.4-V_{pp} input signals the output phase imbalance is as poor as four degrees. If the input signal level is small and close to the critical minimum, then the sensitivity to amplitude error is higher. Correspondingly, with a large input signal level, the sensitivity is less. To summarize this, we can observe that a DFF unit attenuates amplitude errors, but also converts them to phase errors. Phase errors are attenuated with a certain factor, such as five in this circuit. This explains why divide-by-four IQ generation using two

consecutive unity-feedback DFFs is a reasonably good approach if just a modest IQ balance is needed.

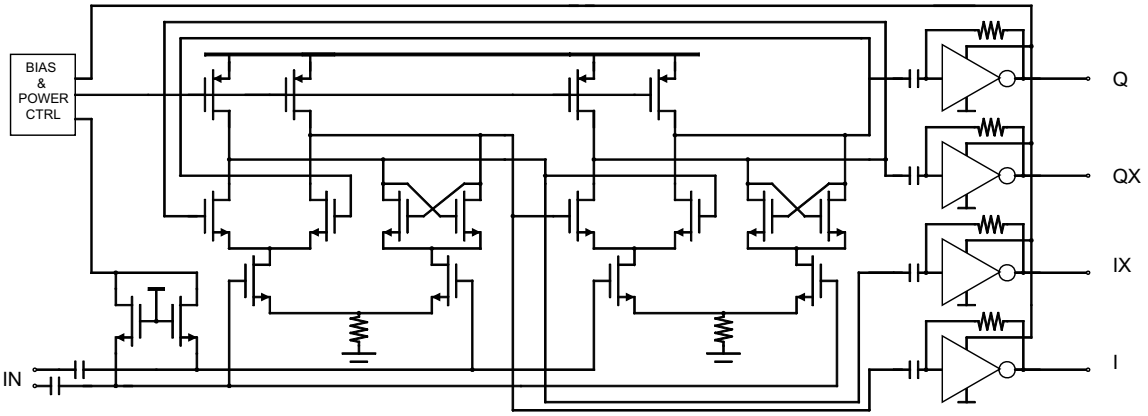


Figure 8.11. Schematic of divide-by-two IQ generator.

8.1.3 Quadrature Oscillators

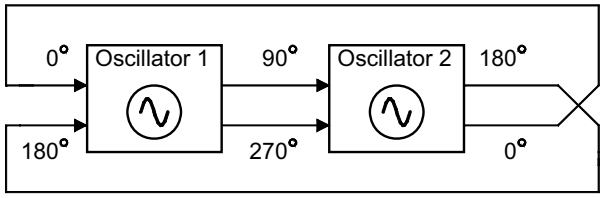


Figure 8.12. Basic principle of quadrature oscillators.

If two differential oscillators are coupled, they may oscillate either in-phase or in quadrature phase. Figure 8.12 depicts how direct and inverted connections should be arranged to force two differential LC oscillators to oscillate in quadrature. In the modern RF IC context this was first proposed in [8.31], although the idea of coupling itself is old [8.32]. The basic coupling arrangement utilized in [8.31] is shown in Figure 8.13a. Since the key principle in quadrature coupling is just to transfer energy between the two oscillators in such a manner that quadrature oscillation takes place, many alternative circuit techniques exist. Razavi improved the original arrangement of parallel coupling by introducing separate current sources for the negative conductance transistors and for the coupling transistors [8.33]. Later, Mazzanti compared these two in detail [8.34]. Lo proposed a modification where the common-source nodes of opposite structures were connected together [8.35]. Tiebout used both NMOS and PMOS pairs for the coupling [8.36]. Van der Tang proposed the use of tunable phase shifters (emitter followers) to reduce phase noise [8.37]. Instead of parallel coupling, active devices can be placed in series. Wu used PMOS loads [8.38] (Figure 8.13b), and Andreani proposed both top-series [8.39] (Figure 8.13c) and bottom-series [8.40] (Figure 8.13d) NMOS device arrangements. A MOSFET back-gate can be used for coupling directly [8.41] (Figure 8.13e), or with the aid of additional transformer [8.42]. Coupling with capacitive source degeneration was used in [8.43] (Figure 8.13f), and feeding the signals into the current sources was used in [8.44],[8.45] (Figure 8.13g). Coupling signals can also be fed to the common-source node [8.46]-[8.48], so that coupling takes place at the second harmonic. Instead of active devices, inductive coupling, often using transformer structures, can be used [8.49]-[8.52].

The key targets in quadrature oscillators are the IQ balance and phase noise, and many analyses of coupling techniques and on the impact of device mismatch have been presented. In addition to analysis carried out in the previous circuit-oriented papers, some good analytical works are

presented in [8.53]-[8.56]. Without going into details, the main message is that regardless of how the mutual quadrature coupling is implemented, there is always some penalty in terms of phase noise, and good IQ balance and the lowest available phase noise level are competing objectives. This means in practice that a quadrature LC-VCO always has worse phase noise than the corresponding single differential oscillator. Design cases where the phase noise requirements are challenging to meet with any reasonable die area and power budget are not that uncommon, and in those cases even the loss of some dBs in phase noise performance is critical. Personally, in project tasks I have ended up not using quadrature LC oscillators for IQ generation. The main reason is that LC oscillators are often one of the most expensive circuits in terms of die area, and the use of quadrature LC-oscillators emphasizes this problem further. The alternatives, polyphase filters and divide-by-two or -four circuits, consume just a small area. Concerning power efficiency, the choice of the best alternative depends on many aspects. If high-Q resonators are available and the tuning range requirement is not excessive, then LC oscillators are power-efficient. It should be kept in mind that one oscillator is needed anyway in alternative methods. Polyphase filters require power-consuming loss compensation, and therefore they become less attractive at higher frequencies. DFFs can be designed for quite low power up to a certain frequency limit set by the applied technology. Excessive power is needed to push the operation above that limit. Thus, the final decision on these three alternatives depends on the required bandwidth, operating frequency with respect to technology, available device characteristics, such as the resonator Q-value or parameter spread, and on specific design targets, such as low power or small area.

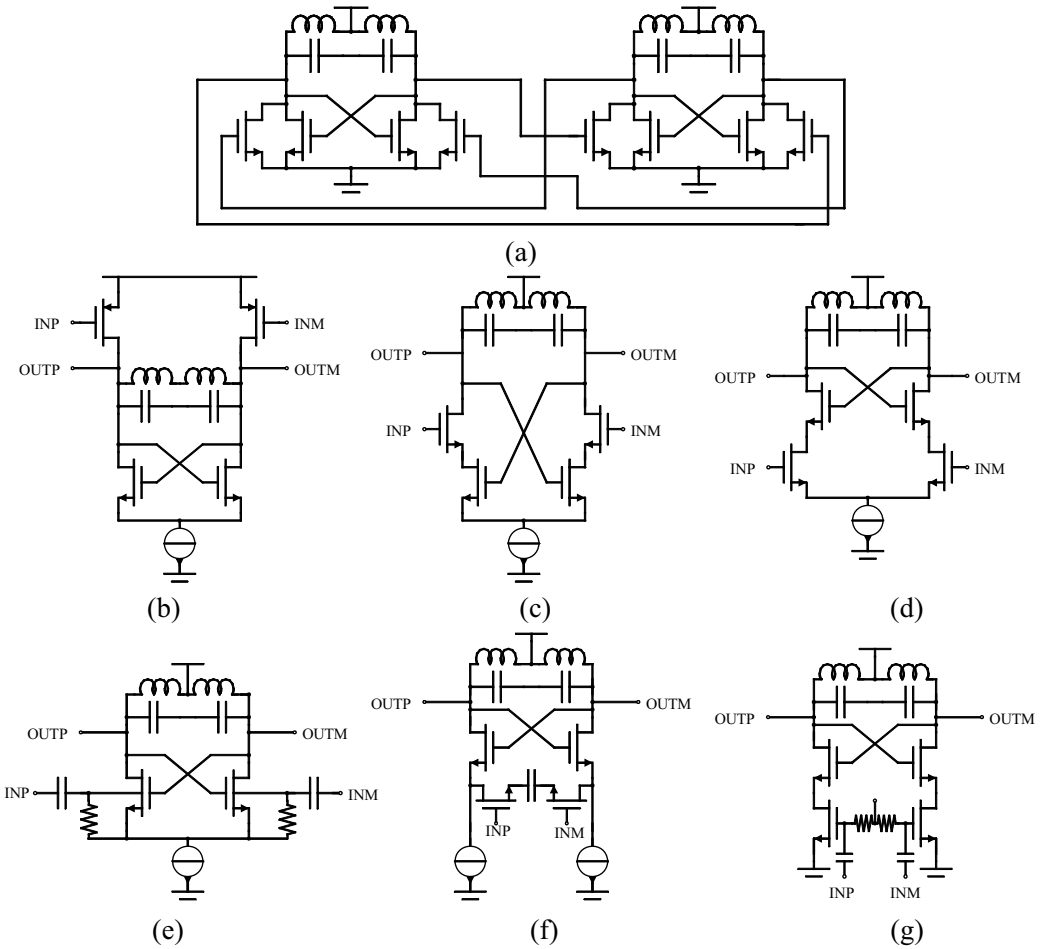


Figure 8.13. Some coupling techniques (a) parallel coupling, both oscillators shown [8.31]
(b) PMOS load coupling [8.38] (c) top-series coupling [8.39] (d) bottom-series coupling [8.40] (e) back-gate coupling [8.41] (f) coupling with capacitive source degeneration [8.43]
(g) coupling with current sources [8.45]

8.2 Frequency Conversion Techniques

A generated oscillation signal can be transferred into another frequency with the aid of specific circuits that are the subject of this section. The four basic arithmetic functions – addition, subtraction, division, and multiplication – can be performed in the frequency domain. There are at least three purposes for frequency conversion. First, one may generate additional frequency bands from a single source. Typical examples are GSM systems at 900 MHz and at 1800/1900 MHz, and the generation of an LO signal for WLAN a/b/g. A single synthesizer can generate both bands with the aid of divide-by-two, or multiply-by-two circuits. Second, one may alleviate unwanted coupling problems. A common example is LO leakage in direct-conversion receivers. The LO signal mixes with itself and generates a constant DC offset. The LO signal may also leak from the antenna, since the preselect filter does not attenuate it. This may disturb other receivers in the vicinity. If the radiated LO signal reflects back, the DC offset may even vary with time. The LO coupling may take place via the substrate, via capacitive paths, and via inductive paths. If the oscillator is designed not to operate in the reception band, and only a small-size frequency conversion circuit provides the actual LO signal, then this coupling issue is greatly relieved. Third, cases may appear where the oscillation frequency range is limited, and then frequency conversion circuits can be used to shift the signal to the desired frequency. This is not that severe an issue in RF ICs, but for instance at very high frequencies it is a common habit to use a lower-frequency oscillator and a frequency multiplier to generate the LO signal. Another example could be a case where a good-quality LO signal is needed at a frequency of some hundreds of MHz. Monolithic coils are then too large and have a low Q-value. An oscillator at a higher frequency and an appropriate frequency divider would be a good solution.

The ever-increasing number of services and telecommunication systems create a demand to establish multi-band multi-mode radio transceivers. For instance, a typical cell phone already on sale today includes at least transceivers for 2G/3G systems, for Bluetooth and WLAN connections, and a GPS receiver. We discussed the related IC design challenges in [8.57]. Here, the first part of this section gives an overview of multi-band LO frequency generation methods, and the later subsections then focus on the actual circuit techniques.

There are four basic methods for multi-band frequency generation.

1) An oscillator with a really wide tuning range could cover the bands of several systems. However, such an oscillator suffers from high phase noise, as discussed in earlier chapters. It is difficult or even impossible to meet the phase noise specification with acceptable power consumption and die area. A wide-tuning-range voltage-controlled oscillator fabricated in a modern silicon technology typically has a 20 – 30 % tuning range, while the best results are almost 50% [8.58],[8.59]. Typically, in fully integrated synthesizers, a VCO includes a switched capacitor network for coarse tuning and a varactor for fine-tuning. Such an arrangement provides the wide tuning range required for wideband operation and immunity to process-voltage-temperature variations, and yet it offers good phase noise characteristics. Switched inductors are a method to extend the frequency range further, but the reported implementations have quite a modest phase noise performance [8.60]-[8.63]. Magnetic tuning, proposed in [8.52], provides a really attractive tuning range, but at least the reported circuit also has quite a modest phase noise performance, though it compares well with other circuits with an equally wide tuning range. In this first category, a VCO provides the desired LO band directly. Examples of this type of frequency generation may be found in [8.6],[8.65],[8.66]. However, to avoid VCO frequency pulling and LO-RF interaction, particularly in direct-

conversion and low-IF receivers, it is preferable to have the VCO at a different frequency from the actual reception band. Therefore, this direct method is not often favored.

2) An extension to the first category is to use a set of parallel VCOs (a VCO bank). Such a VCO group can cover several frequency ranges; see, for example, [8.66]. The main drawback is a significantly increased die area. However, now each VCO can be tailored for a good phase noise – power consumption – tuning range trade-off. The unique VCO tuning gain K_{VCO} [MHz/V] requires some reconfigurability / tunability from the rest of the phase-locked loop. In the simplest case tuning the charge pump current is sufficient.

3) The VCO oscillates at a multiple of the desired frequency and the actual LO signal is generated with a frequency divider. By having several parallel dividers with different division ratios or a configurable divider, it is possible to generate different bands. The method is tempting, since it offers the freedom to generate a large quantity of bands and the VCO coupling problem is alleviated. At high frequencies, the VCO coil is also smaller, and since the dividers are tiny devices, this is a small die area approach. This method is most commonly implemented using divide-by-two and divide-by-four circuits; see e.g. [8.67]-[8.74].

4) A fractional relation between the VCO and LO frequencies can be generated with the aid of a frequency divider and a single-sideband mixer or a plain mixer with image sideband filtering; see e.g. [8.75]-[8.79]. The fractional relation relieves the coupling and interference problems and, in general, provides freedom in reception frequency planning. On the other hand, single-sideband mixers have moderate image rejection, while the unwanted tone leaking to the LO port results in undesirable mixing products, which can corrupt reception [8.76]. In addition, these structures are quite complex and signal levels are attenuated in the mixing or post-filtering. Thus, some amplification is needed and power consumption tends to increase. Finally, a plain mixer can be used as a multiply-by-two element for multi-band creation [8.80],[8.81].

The RF portion of a multi-mode frequency synthesizer can include more than one of these approaches. Figure 8.14 depicts a general view of all four proposed methods. Further modifications can include the addition of another VCO in parallel, thus doubling the bands. Some multi-mode synthesizers utilizing combinations of these methods are presented in [8.79]-[8.82].

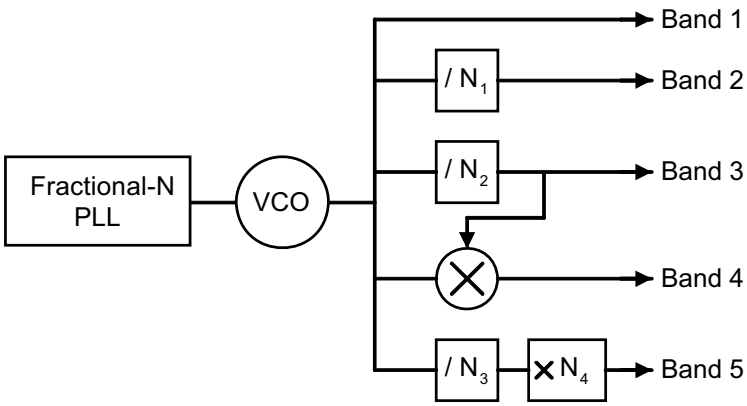


Figure 8.14. Generic diagram for multi-band LO generation. N refers to an appropriate integer.

8.2.1 Addition and Subtraction in Frequency Domain

Addition and subtraction functions in the frequency domain can be accomplished with an analog multiplier circuit, commonly called a mixer. The two prevailing mixer circuit categories are the current-steering circuit, i.e. the Gilbert cell, and the passive resistive mixer. The mixer can actually be constructed from any nonlinear device. As far as this discussion is concerned, all mixers share the same main properties, and the exact circuit arrangement is an irrelevant topic here.

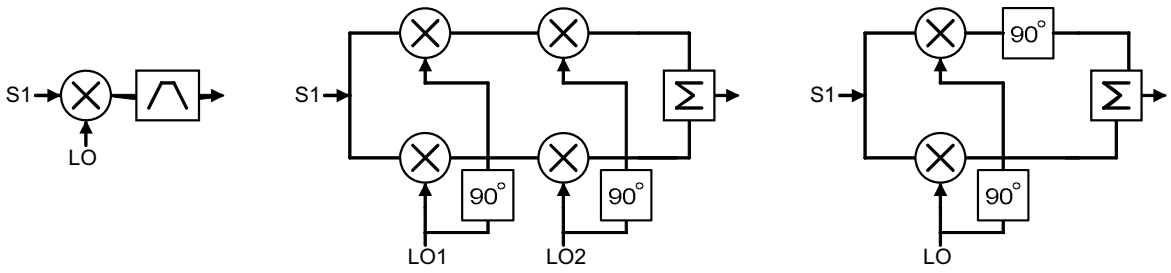
Consider two signals with a third-order distortion

$$\begin{aligned} S_1 &= \sin\omega_1 t + A_3 \sin\left(3\omega_1 t + \alpha_3\right) \\ S_2 &= B_1 \sin\left(\omega_2 t + \beta_1\right) + B_3 \sin\left(3\omega_2 t + \beta_3\right) \end{aligned} \tag{8.8}$$

The product of these two is

$$\begin{aligned} S_1 \times S_2 \quad = \quad & \tfrac{1}{2} B_1 \cos\left(\omega_1 t - \omega_2 t - \beta_1\right) - \tfrac{1}{2} B_1 \cos\left(\omega_1 t + \omega_2 t + \beta_1\right) \\ & + \tfrac{1}{2} B_3 \cos\left(\omega_1 t - 3\omega_2 t - \beta_3\right) - \tfrac{1}{2} B_3 \cos\left(\omega_1 t + 3\omega_2 t + \beta_3\right) \\ & + \tfrac{1}{2} A_3 B_1 \cos\left(3\omega_1 t - \omega_2 t + \alpha_3 - \beta_1\right) - \tfrac{1}{2} A_3 B_1 \cos\left(3\omega_1 t + \omega_2 t + \alpha_3 + \beta_1\right) \\ & + \tfrac{1}{2} A_3 B_3 \cos\left(3\omega_1 t - 3\omega_2 t + \alpha_3 - \beta_3\right) - \tfrac{1}{2} A_3 B_3 \cos\left(3\omega_1 t + 3\omega_2 t + \alpha_3 + \beta_3\right) \end{aligned} \tag{8.9}$$

The message here is that even with ideal multiplication we get many output tones. They are not caused by circuit non-idealities. In LO generation only one of these is the wanted one, and the rest should be suppressed. The spectrum is symmetric and we may attenuate one side of the spectrum with filtering or with complex mixing. The three alternatives are depicted in Figure 8.15. In RF ICs filtering with sufficient attenuation is difficult to achieve. In Weaver's method [8.83] the problem is the second image caused by the second mixing [8.3]. It will leak through without any attenuation thus spoiling the spectral purity. The Weaver topology also requires complicated circuit arrangements, and therefore single-sideband (SSB) mixing is usually implemented with the Hartley topology. In Hartley's method three issues limit the actual achievable image rejection. One is the quality of the summing circuit, the second one is imperfect phase and amplitude balance of the input signals, and the third is device mismatch inside each mixer. The summing circuit is almost exclusively implemented as a polyphase filter. Switching the polarity of one input signal (LO signal in the receiver context) results in the possibility of changing the attenuation of upper or lower sideband in a simple manner [8.84]. Here such a circuit will be marked with SSB-U/L. For system-level considerations an SSB mixer is characterized by properties such as conversion gain, LO leakage, RF leakage, image rejection, and power and area consumption. In a typical RF IC implementation SSB mixers are far away from their ideal behavior. Leakages and moderate image suppression result in the output spectrum being contaminated with a plurality of tones. In transceivers such a dirty LO signal results in unwanted interfering tones being converted into the same band as the actual signal, and the signal is therefore corrupted. Figure 8.16 presents a simple sketch for the generation of a tunable LO with the aid of an SSB mixer. It also depicts where the spurious tones appear. In this concept the high-frequency source f_{HF} is tuned in very coarse steps and the low-frequency source f_{LF} provides the fine-tuning, so that the resulting f_{LO} is tuned over a very wide frequency range in small increments. The method requires two frequency synthesizers, one at a high frequency and another at a slightly lower frequency. Furthermore, the final output will include unwanted tones, and therefore this scheme is not generally accepted.



(a) (b) (c)

Figure 8.15. Single-sideband mixers: (a) image filtering (b) Weaver (c) Hartley.

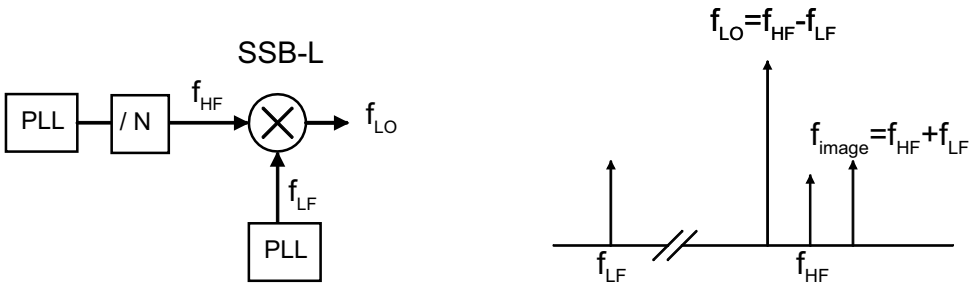


Figure 8.16. One sketch of how to use a single-sideband mixer to generate a multi-band LO signal. On the right, the main output tones are shown. Each tone has its higher harmonics as well, so the overall spectrum includes many weaker tones not shown here.

8.2.2 Frequency Multipliers

Frequency multiplication can be done with several different circuit techniques. These are based on three principles: harmonic generation in a nonlinear device, analog multiplication, or injection locking. Furthermore, in digital circuits an XOR-gate and a quarter-period delay are used to generate a double-rate digital signal. Prior to discussion on the actual circuits, it is useful to do some simple trigonometric calculus.

First, let us multiply two sinusoidal signals.

$$\left.\begin{aligned} S_1 &= A_1 \sin \omega t \\ S_2 &= A_2 \sin\left(\omega t + \theta\right) \end{aligned}\right\} \Rightarrow \; S_1 \times S_2 = \frac{A_1 A_2}{2}\left(\cos\theta - \cos 2\omega t \cdot \cos\theta + \sin 2\omega t \cdot \sin\theta\right) \tag{8.10}$$

Three cases are of particular interest. If two equal signals are multiplied, i.e. θ=0, then we get a double-frequency output and a DC shift. If θ=90°, then the DC term vanishes. Finally, if θ=45°, we do not have any signal at all. This means that small phase deviations from θ=0° or θ=90° result in a lower conversion gain. Furthermore, a fundamental property in multiplication is that two signals are converted into one.

Next, let us consider another simple case where we multiply two equal signals that have second-order harmonics.

$$\left[A \sin \omega t + B \sin\left(2\omega t + \theta\right)\right]^2 =$$

$$\frac{A^2 + B^2}{2} + AB\cos\left(\omega t + \theta\right) - \frac{A^2}{2}\cos\left(2\omega t\right) - AB\cos\left(3\omega t + \theta\right) - \frac{B^2}{2}\cos\left(4\omega t + 2\theta\right) \tag{8.11}$$

The presence of the second harmonic results in the fundamental tone leaking through. If we put two frequency multipliers in series, then the input for the second one includes the leakage of the fundamental, and when multiplied again the sub-harmonic tones appear at the output. This type of mathematical analysis can be further extended to find out other fundamental principles of frequency multiplication. However, the related formulas become overly lengthy and complicated to present here.

Harmonic Generation

The most traditional frequency multiplication technique is to feed a signal through a nonlinear device and thereafter apply an impedance-matching network or a filter to select the desired harmonic. See e.g. [8.85] for discussion of GaAs MESFET frequency doublers. In RF IC implementations matching or filtering elements with sufficient selectivity are not available, and therefore this method results in the fundamental and other generated tones leaking to the output as well. In a balanced configuration the outputs of two nonlinear devices are connected together and if such an arrangement is driven with a differential signal, then the odd harmonics cancel at the output, and only the even harmonics remain. In practice, the fundamental rejection depends on the amplitude and phase balance of the input signals and on the matching of the two devices. Figure 8.17 depicts various circuit arrangements based on this principle. Bias connections are not depicted, but with them the devices are usually biased close to class B. Cases (a) [8.86] and (b) [8.87] are the basic arrangements, but suffer from single-ended output. A common technique to perform the single-to-differential conversion in RF ICs is to operate a single transistor simultaneously in common-source and common-drain modes. The same idea is applied for a multiplier in Case (c) [8.88]. Unfortunately, output signals have severe amplitude and phase mismatch. Both PMOS and NMOS pairs can be combined as shown in Case (d). This arrangement has good conversion efficiency, but it also suffers from single-ended output. One solution [8.89], shown in Figure 8.17e, is to add an LC-resonator. This structure is, unfortunately, narrowband in nature and the coil consumes a large die area. All circuits based on harmonic generation tend to have low conversion gain, and thus poor power efficiency.

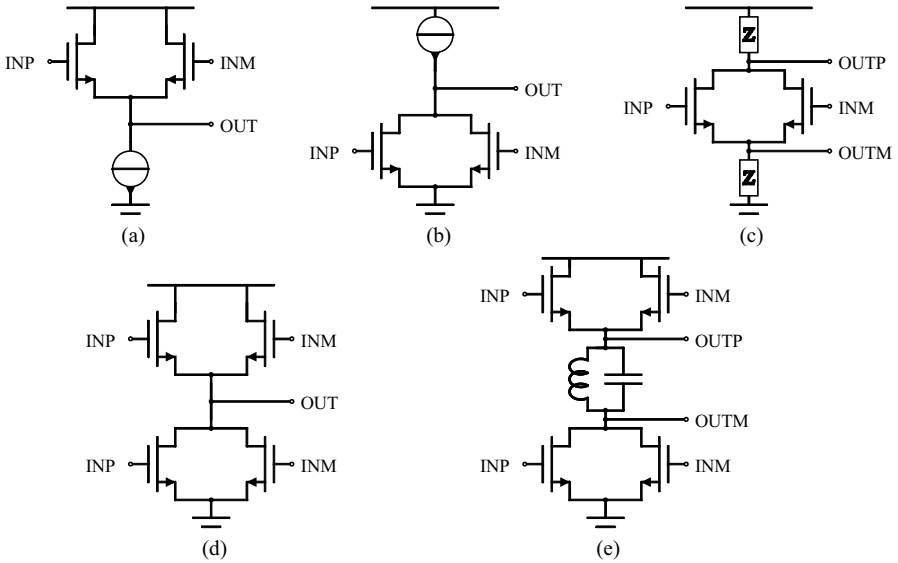


Figure 8.17. Some multiply-by-two frequency multipliers based on harmonic generation.

Analog Multipliers

In an RF IC context analog multipliers, such as the Gilbert cell, passive mixer, or a multiplier based on asymmetric source-coupled pairs [8.90] (see Figure 8.30) can be used for frequency

multiplication as well, but they do suffer from some drawbacks. First of all, as we learnt from the math done above, the output signal is not differential anymore. This is not an obvious issue just from looking the schematic, at least not for me. Second, if the input signals are just differential, but not in quadrature, then the output has an input-level related DC offset. This results in the conversion gain being quite nonlinear, and somewhat difficult to predict accurately. Therefore, for instance in [8.91], [8.92], poly-phase filters are used to generate the four-quadrant input signals.

Injection Locking

In differential oscillators, such as in the cross-coupled pair based circuits, the common-source node has even-mode harmonics, actually just like in Figure 8.17a. Frequency multiplication by two can be done by injection locking an oscillator at the fundamental frequency, and taking the output from the common-mode node. If a two-stage structure is used, then the outputs are differential [8.26]. If a four-stage structure is used, then we have quadrature outputs and mixers can be used to establish a multiply-by-four circuit [8.93].

Edge Combining

With the aid of a delay-locked loop (DLL) we may generate a set of rising and falling edges accurately. Then an edge-combining circuit changes its output state every time a rising or falling edge appears at any of its inputs. The circuit principle and timing diagram are shown in Figure 8.18. The DLL-multiplier multiplies by the number of the delay stages. One may design a circuitry, where the number of delay stages and the corresponding edge-combiner can be selected, and hence has a tunable multiply-by-integer circuit. Delay-locked loops have a feedback path that is used for fine-tuning the unit delays. Hence, on the circuit block level they resemble phase-locked loops, and DLL-based frequency synthesizers are therefore quite complicated frequency multipliers, in contrast to the previous circuits. Some good works utilizing edge combining are presented in [8.94]-[8.98].

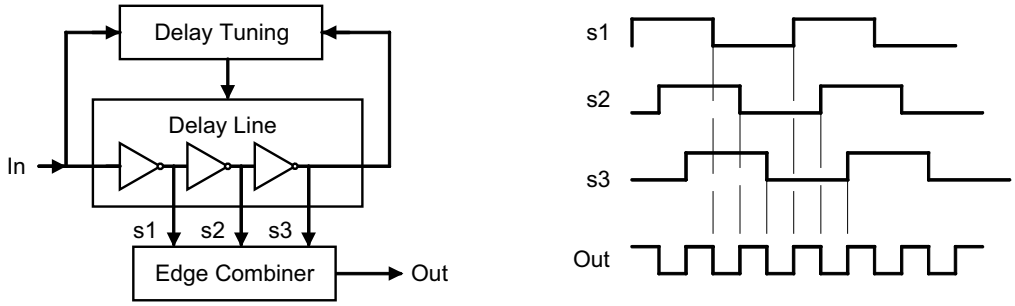


Figure 8.18. Delay-locked loop on the left, and its timing diagram on the right.

8.2.3 Frequency Dividers

Two types of analog frequency dividers are occasionally used. Miller dividers were already discussed briefly. Injection-locked oscillators acting as frequency dividers suffer from a narrow locking range. They may have potential in some specific cases as a low-power method. The vast majority of RF IC frequency dividers are based on digital-type circuits – namely D-flipflops. In this context we focus on those. Dividers are based on a counter principle. A circuit counts the input signals up to an integer N, and then outputs a signal, and the cycle repeats itself. The output signal is the input divided by N. One may modify the counter not to go through all the logic states with a specific arrangement of some additional logic elements. In this way the base counter can be altered to divide by a smaller integer.

Binary dividers (divide-by-2^N) are constructed from N D-flipflops arranged into an asynchronous chain. Such a divide-by-8 circuit is shown in Figure 8.19a. Case (b) shows the basic synchronous counter, the Johnson counter. It divides by 2N, so the four-DFF unit that is depicted also divides by eight, and a three-DFF counter in Case (c) divides by six. In Case (a) each consecutive flipflop runs at twice as low a frequency. Power is saved and the input has high impedance. However, now each DFF acts independently and that causes increased timing inaccuracy (jitter). This jitter accumulation in a long chain can be avoided by adding one flipflop clocked with the input signal at the end of the chain [8.99]. In Case (b) the input signal clocks all the flipflops, and therefore they all run at a high frequency. This consumes a lot of power, and the input represents a low-impedance load requiring a strong input driver. The decision on how to group dividers in a divider chain thus depends on the power budget, noise issues, and the divider input driver characteristics. At different frequencies, with respect to the technology applied, this choice may vary a lot. As said, basic counters can be altered to a divider with the desired division count by adding the proper logic. In the prescalers used within PLLs, dual-modulus dividers are a common method used to establish an eventual fractional division count. Various structures have been proposed during the years; see e.g. [8.100]. As an example, one divide-by-4 or by-5 circuit is depicted in Figure 8.19d. In LO-generators we may use these circuits and simplify them by removing the modulus control. Furthermore, OR/NOR gates should be preferred since they reduce the maximum toggle frequency less than AND/NAND circuits. Case (e) depicts how the NOR-port is used to convert a divide-by-four circuit into a divide-by-three circuit [8.101]. The additional logic gate can be embedded into the DFF cell, and the complexity increment is not as high as one might expect. For instance, the NOR-gate can be embedded into a D-flipflop by adding just one additional transistor [8.101],[8.102]. Therefore, Case (e) actually includes two NOR-DFF cells, and although one of the NOR-cells is hardwired, it makes sense to keep it there.

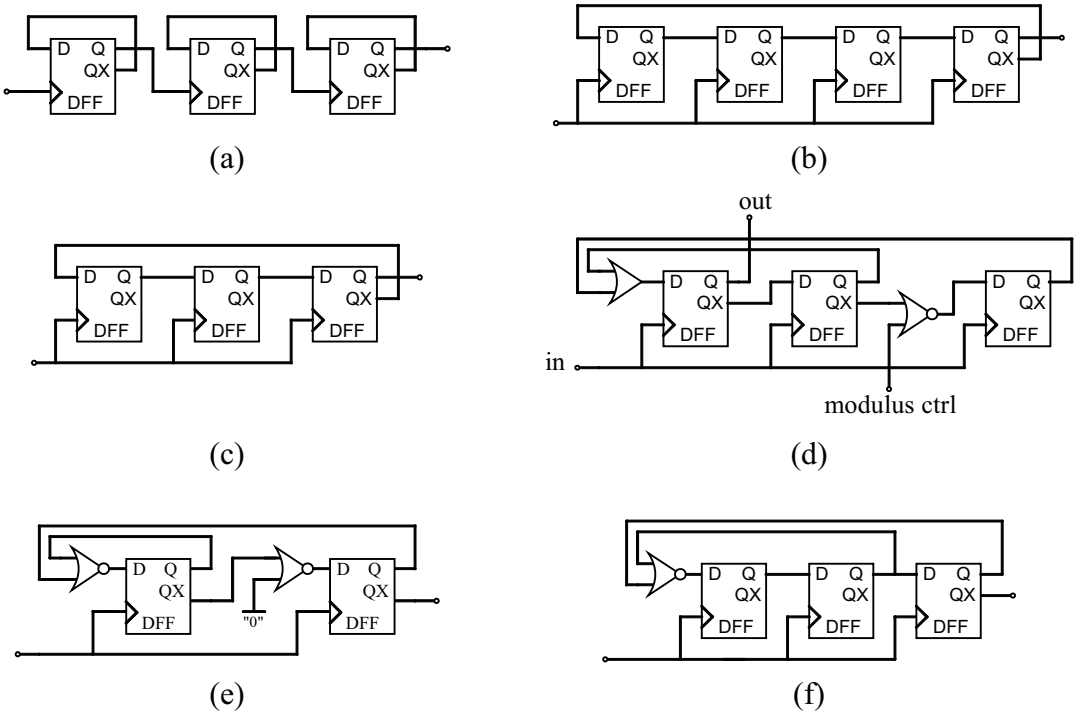


Figure 8.19. DFF-based frequency dividers (a) asynchronous divide-by-8 (b) synchronous divide-by-8 (c) divide-by-6 (d) dual-modulus divide-by-4/5 (e) divide-by-3 (f) divide-by-5. Note that although the signals are here drawn as single-ended, in SCL DFF designs signals are all differential.

When the division count differs from the binary count, then in general the output duty cycle is no longer 50%. For instance, the divide-by-three circuit in Figure 8.19e has a duty-cycle of 1/3. DFF-based circuits are edge-triggered and they cope well with an input signal that has a non-50% duty cycle. Mixers can also operate at different LO duty cycles. We studied this issue when designing a cognitive radio front-end [8.30], and found out that a 50-% duty cycle square wave is the best choice for high gain and linearity. Basic analog circuits, such as a differential pair, do not work well with a non-50% duty cycle signals. Furthermore, a non-50% duty cycle corresponds to an output spectrum with some spurious tones. Hence, the output duty cycle from a frequency generation unit should usually be 50%. One technique to produce 50% output duty cycle, or to achieve a non-integer division count, is to modify the divider output signals with some additional logic gates [8.103],[8.104]. A divide-by-three circuit with additional logic is shown in Figure 8.20.

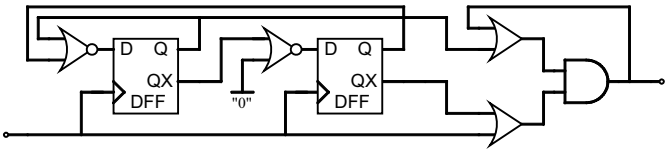


Figure 8.20. A divide-by-three circuit with additional logic gives a 50-% output duty cycle.

DFFs may be designed to toggle the logic state with either a rising or falling edge of the input signal. An extension is to have a DFF that can be triggered on either the rising or falling edge depending on the setting of a control input. I will call such a device up/dw-DFF. By selecting the triggering edge with a signal present in a divider chain, we may generate odd division counts, or even more interestingly, division counts of N+½. In [8.91] three phase-switchable DFFs were used for a divide-by-three circuit that had a 50-% output duty cycle. The ECL DFFs were extended by adding a row of transistors for phase switching functionality. In [8.105] the same idea was applied. In [8.106] two parallel D-latches and a MUX-circuit were used to establish an up/dw-DFF. The authors constructed a divide-by-5½ divider. Lee and Huang used an up/dw-DFF in a divide-by-7½ circuit [8.107]. They added the additional control switches below the clocking transistors in an SCL DFF cell. In addition, a “semi-dynamic” divider circuit – a Miller divider including a digital divider – was presented in [8.108], and it can divide by 2½.

I applied the up/dw-DFF structure proposed by Lee and Huang to implement a divide-by-1½ circuit, and a divide-by-three circuit with a 50-% output duty cycle. The work was related to the UWB project, which will be discussed in Sections 8.3 and 9.5. Figure 8.21 depicts the cell-level arrangement and the structure of the latch within the up/dw-DFF. The transistor-level behavior of this circuit is very close to that of a conventional SCL DFF, and hence I will not present the simulation details here. These units were used for designing two complete divider chains, presented in Figure 8.22, with division counts of 13½ and 15. The circuits are designed with a 65-nm CMOS process. According to simulations, the divide-by-13½ circuit operates with a 9-GHz input frequency in all process corners, consumes 5 mA from a 1.2-V supply, and delivers an output signal with a 50-% duty cycle. The divide-by-15 circuit operates also with a 9-GHz input frequency, consumes 4 mA from a 1.2-V supply, and delivers an output signal with a 50-% duty cycle.

To summarize the discussion on frequency dividers, we may say that in practice a 50-% output duty cycle is required from a frequency divider chain. Divide-by-2^N circuits have such an output naturally, and other circuits with integer division counts that produce such signals can be designed with the methods that were discussed. Moreover, circuits with non-integer division counts do exist. Specifically, here I used divide-by-1½ and divide-by-7½ circuits. In general,

the same techniques as those discussed here can be exploited to generate other integer and N+½ division counts.

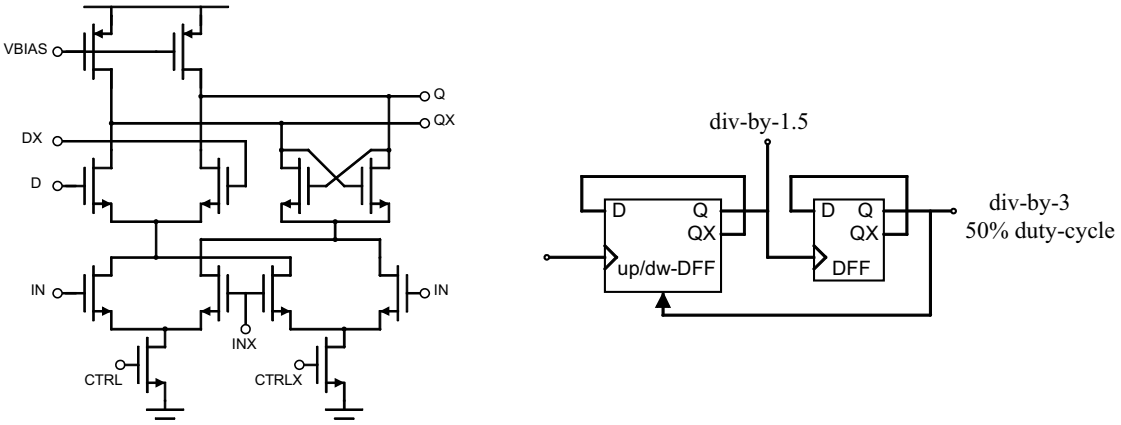


Figure 8.21. up/dw-DFF latch structure, where the CTRL signal sets the triggering to the rising or falling edge of the input signal. A divide-by-1½ and by three circuit is shown on the right.

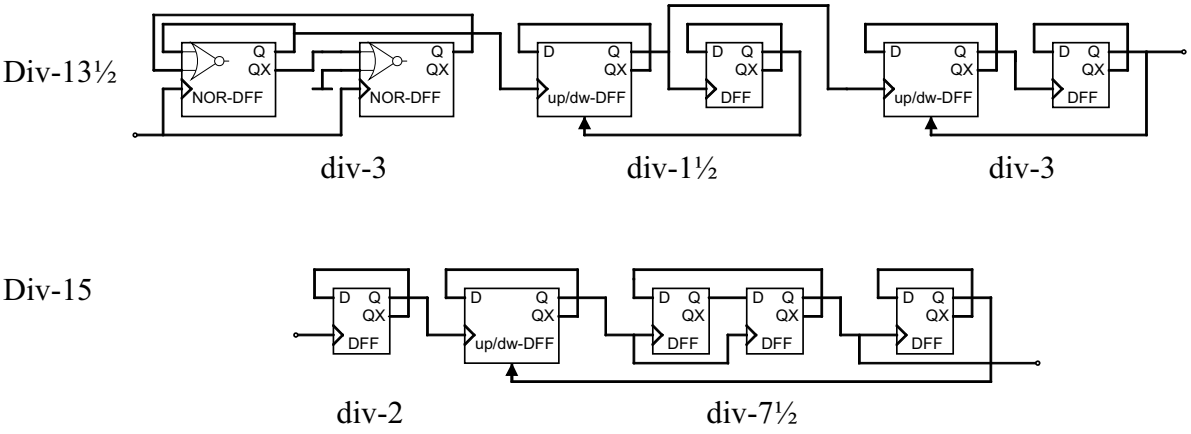


Figure 8.22. Divider chains including some non-common divider units.

All in all, this section included a brief discussion on how to perform frequency conversion for a signal. The four basic mathematical operations can be performed in the frequency domain, but only the divider circuits are free of major problems. Multipliers have poor power efficiency, and unwanted tones appear at the output. It is beneficial to have the input signals in quadrature, but, as is known, such signals are not always available and quadrature generation poses its own challenges particularly regarding the frequency range. Single-sideband mixers also suffer badly from an impure output spectrum. They often consume a lot of power and require complex circuit arrangements. In general, frequency conversion circuits are powerful tools for increasing the frequency range of a frequency synthesizer, and they ease the frequency planning of a transceiver. Because of their usefulness on one hand, and on the other hand the design challenges they pose, frequency conversion circuits and methods are a fruitful field for research and future innovations.

8.3 SSB Mixing Method for UWB Synthesizer

This section deals with a design case where I studied techniques for LO-signal generation for ultra-wideband (UWB) radios, and developed an SSB mixing based method for that. Later, in Section 9.5, actual circuit implementations based on three parallel PLLs for the same purpose are presented.

Ultra-wideband (UWB) communication systems have been considered as a potential technology for short-range high data-rate applications. In the U.S. the Federal Communications Commission (FCC) made the 3.1–10.6 GHz frequency range available for UWB applications and thereafter several system proposals were considered within the IEEE workgroup 802.15 [8.109]. The Wimedia – formerly known as the Multiband OFDM Alliance (MBOA) – UWB proposal has evolved into an industrial standard, ECMA-368 [8.110]. That system uses multi-band orthogonal frequency division multiplexing (MB-OFDM). The radio spectrum is divided into bands that are 528-MHz wide, which are further bound into band groups (BG) as shown in Figure 8.23, and also listed in Table 8.1. As a plan for the first products, band group 1 was defined as the mandatory one and band group 3 was an extension. Band group 2 was left unused since it overlaps with the 5-GHz systems, such as WLAN. Higher band groups were reserved for future use as the technology matures. In the newer version of the ECMA-386 standard, there are no specific mandatory band groups. However, the work presented in this thesis is based on the early WiMedia proposal. In the ECMA-368 standard the symbol interval is 312 ns and frequency hopping from band-to-band within one band group takes place after each symbol. There is a 9-ns guard period between the symbols. This very fast frequency-hopping rate is beyond the requirements of any previous systems. It turns out that conventional PLL-based frequency synthesizers are not able to settle into the new frequency fast enough. The settling requirement for the dual-PLL concept, where one PLL is active and the inactive one is settling towards the next frequency, is the length of one symbol. With present PLL know-how such a settling speed is not attainable while maintaining adequate noise characteristics, low power consumption and small die area. Batra et al. from TI proposed a mixing-method based approach for generating a fast frequency-hopping LO-signal [8.111], [8.112]. In this method a set of different fixed frequencies is generated with the aid of conventional PLL and frequency dividers, and then single-sideband mixers and switches are used to generate the desired LO tone. Here we review Batra's original proposal and point out some problems associated with that arrangement. Then a simple mathematical formulation is presented, which leads to improved and simplified structures.

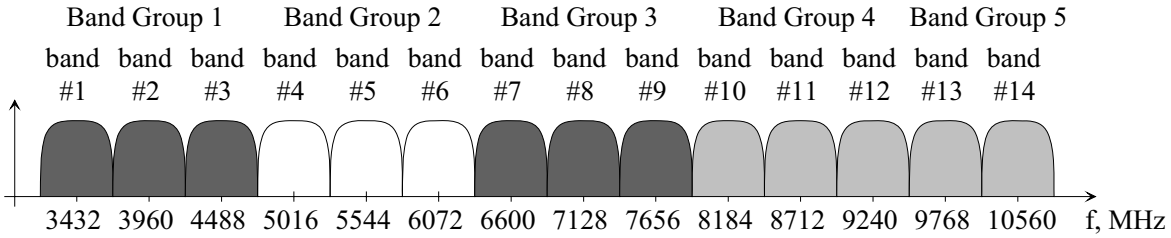


Figure 8.23. WiMedia UWB band allocation. The LO-tones for the dark shaded band groups one and three are the target of the developed circuit.

Table 8.1. WiMedia UWB band allocation and the main SX requirements.

Band Group	Band ID	Frequency band [MHz]	Center Frequency [MHz]	
1	**#1**	**3168−3696**	**3432**	**6.5 fr**
	#2	**3696−4224**	**3960**	**7.5fr**
	#3	**4224−4752**	**4488**	**8.5fr**
2	#4	4752−5280	5016	9.5fr
	#5	5280−5808	5544	10.5 fr
	#6	5808−6336	6072	11.5 fr
3	**#7**	**6336−6864**	**6600**	**12.5 fr**
	#8	**6864−7392**	**7128**	**13.5 fr**
	#9	**7392−7920**	**7656**	**14.5 fr**
4	#10	7920−8448	8184	15.5 fr
	#11	8448−8976	8712	16.5 fr
	#12	8976−9504	9240	17.5 fr
5	#13	9504−10032	9768	18.5 fr
	#14	10032−10560	10296	19.5 fr

Raster frequency f_r = 528 MHz

Hopping rate 3.2 MHz

Guard period 9 ns

The TI's proposal from [8.111], [8.112] is depicted in Figure 8.24. With a PLL-based a synthesizer $8 \cdot f_r$ (4224 MHz) tone is generated. The symbol f_r refers to a raster frequency of 528 MHz. A frequency divider chain and a single-sideband mixer are then used to generate the tones $0.5 \cdot f_r$ and $1.5 \cdot f_r$. With another single-sideband mixer, including a selection for upper/lower sideband rejection, one LO tone within band group one is generated. The proposed method inherently allows fast switching, since all the frequencies are readily available. However, it has a fundamental problem. Because of imperfect SSB mixing and the signal harmonics generated by digital frequency dividers, the output spectrum is contaminated with a large quantity of tones. These unwanted tones are inextricable from the desired LO tone. Spurious tones act like an LO for the UWB signal producing replicas into other bands. In addition, strong out-of-band interferers are converted into bands of interest. Thus, in order to maintain adequate signal quality, the output signal that is generated should have a low content of spurious tones. System simulations for this arrangement reveal that the main causes of spurious tones are the limited SSB mixer image rejection and the harmonic impurities of the signals entering the SSB mixer.

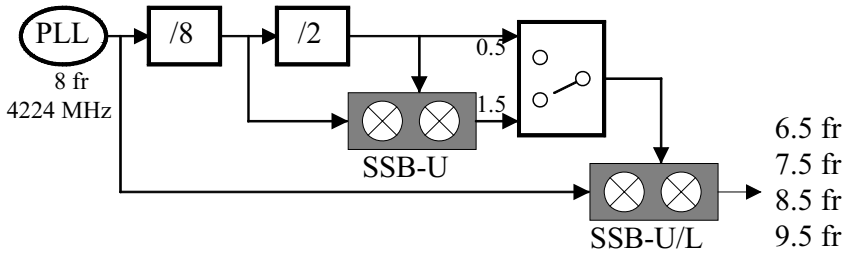


Figure 8.24. TI's reference proposal for UWB frequency synthesis.

The TI's arrangement in Figure 8.24 has several drawbacks. First of all, it generates only band group one frequencies, and our primary objective was to create a system able to produce both BG1 and BG3 frequencies. Second, high spectral purity for the low-frequency mixing components (0.5·fr or 1.5·fr) is required for low spurious content at the output. Differential circuit techniques take care of the even harmonics and therefore the attenuation of the third harmonic is the main topic. Since filtering at this frequency range is particularly problematic, the second objective was to develop a system where only one RF filter is needed. Furthermore,

the reference system includes two SSB mixers, thus consuming a lot of power and occupying a large die area. The probability of inadequate rejections of image and RF and LO leakage is increased and the idea of using automated post-tuning for a high performance SSB mixer is unattractive for two separate units. Therefore, the third objective was to develop a system with only one SSB mixer.

There are four different basic approaches to generating multiples of raster frequency f_r that fit the frequency plan of the WiMedia UWB system. One may start from an integer N, or from N+½, and then add or subtract an appropriate smaller value. Alternatively, the starting point can be a small value, and large ones are added or subtracted. These methods can be expressed mathematically as

Principle 1:	N ± 0.5, 1.5, 2.5, 3.5 etc.	
Principle 2:	N.5 ± 0, 1, 2, 3 etc.	(8.12)
Principle 3:	0.5 ± N, N+2, N+4, N+6 etc.	
Principle 4:	1 ± N.5, N.5+2, N.5+4, N.5+6 etc.	

Here N is an appropriate constant integer. The fact that we are using the "±" operator indicates that an SSB mixer with selectable upper/lower sideband rejection will be used. The TI's method was based on Principle 1, and is {8±0.5,1.5}. To be able to generate band group one and three LO frequencies, we have several alternatives based on the above principles. Some cases can be expressed as

Case 1a:	10 ± 1.5, 2.5, 3.5, 4.5	
Case 1b:	6 / 12 + 0.5, 1.5, 2.5	
Case 2:	10.5 ± 2, 3, 4	(8.13)
Case 3:	0.5 ± 6, 6+2, 2*6, 2*6+2	
Case 4:	1/0 ± 7.5, 13.5	

Cases 1a, 1b, and 2 have several low-frequency mixing components, and each of them requires its own filter. On the other hand, Cases 3 and 4 result in a simpler system concept. Figure 8.25 depicts an arrangement related to Case 3. Here $12 \cdot f_r$ is used as a basic frequency and the high-frequency mixing tones $6 \cdot f_r$, $8 \cdot f_r$, $12 \cdot f_r$, and $14 \cdot f_r$ are generated using frequency dividers. The system is able to frequency-hop in all six bands. Unfortunately, two SSB blocks and two filters are needed, and the concept is not attractive. An arrangement corresponding to Case 4 is shown in Figure 8.26. Here, only one filter and one SSB block are needed. In the WiMedia UWB proposal frequency hopping takes place only inside one band group at a time, and therefore here a single PLL is enough. If hopping should take place within both band groups simultaneously, then two PLL's would be needed. I originally filed the idea shown in Figure 8.26 as an internal invention report in 2004, and it finally evolved into a U.S. patent [8.113].

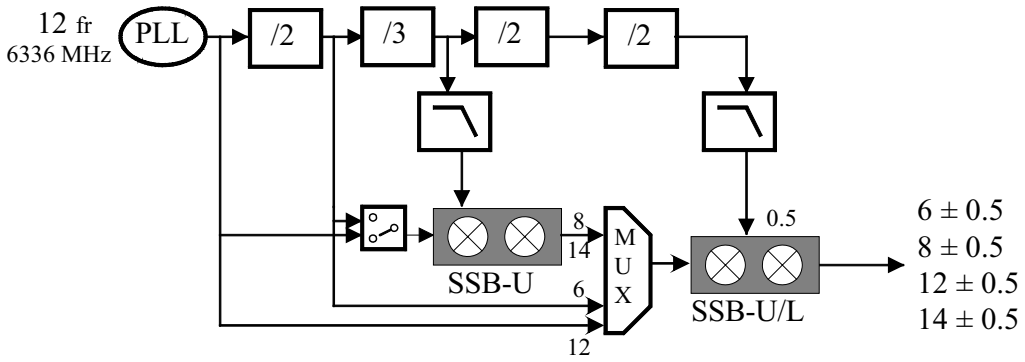


Figure 8.25. System block diagram based on Equation 8.13, Case 3.

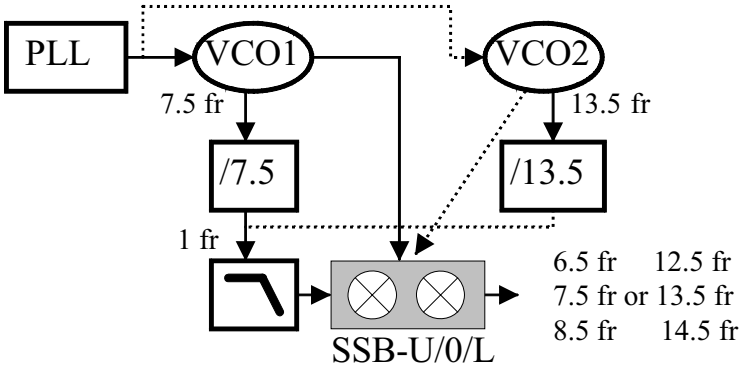


Figure 8.26. My proposal for a UWB LO generator. It is based on Equation 8.13, Case 4.

Two circuit design challenges deserve some attention here. The system proposed in Figure 8.26 includes dividers with the non-common division ratios of 7½ and 13½. These division ratios can be partitioned as

$$\frac{1}{7.5} = \frac{1}{5}\cdot\frac{1}{1\frac{1}{2}} = \frac{1}{5}\cdot\frac{1}{3}\cdot 2 \qquad \textit{and} \qquad \frac{1}{13.5} = \frac{1}{9}\cdot\frac{1}{1\frac{1}{2}} = \frac{1}{3}\cdot\frac{1}{3}\cdot\frac{1}{3}\cdot 2 \tag{8.14}$$

So, the divider circuits discussed in Section 8.2.3 can be used here. We can either directly divide down with divide-by-1½, -5, and -9 circuits, or alternatively the multiply-by-two can be done by taking the second harmonic of the signal of the oscillator from the common-source node of a differential LC-VCO circuit. Then the divide-by-3 and by-5 structures can be used. On the other hand, if we want to avoid the use of these somewhat challenging dividers, then a solution is to generate the $1\cdot f_r$ signal with a completely different method. This signal is also used as a sampling clock for other entities in a UWB radio, and hence it needs to be generated anyway. One technique could be to use a 66-MHz reference signal and a multiply-by-8 DLL circuit. The specific strength of the proposed LO generator is that it includes only one filter, and that one is at a fixed frequency. Since all the signals in the LO generator are differential, the main issue in RF filtering is to attenuate odd harmonics, particularly the third one. Precise circuit design, though, is needed to ensure good symmetry in the layout, as well as low device parameter spread for maintaining high common-mode rejection and a low content of even harmonics. The only filter is in the $1\cdot f_r$ path and the corner frequency for the low-pass filter is at 0.6 GHz. A combination of a LC notch at $3\cdot f_r$ and a low-pass RC filter provides 30-dB attenuation relative to the fundamental frequency for the third harmonic.

The preliminary transistor-level circuit simulations for the proposed system indicated a sufficiently low power consumption and die area. Since the signals at the inputs of the SSB mixer are continuously present and constant, the switching speed is limited only by the inertia of the mixer itself. Figure 8.27 shows a simulated transition from band #9 (7656 MHz) to band #8 (7128 MHz), and the switching time is just about 2 ns. Unfortunately, the simulations also revealed that the spectral purity would remain at best in a level of about -40 dBc. The target was set for much better spectral purity and therefore we did not implement this idea. Instead, we chose to go with three parallel PLLs. That work is described in Section 9.5.

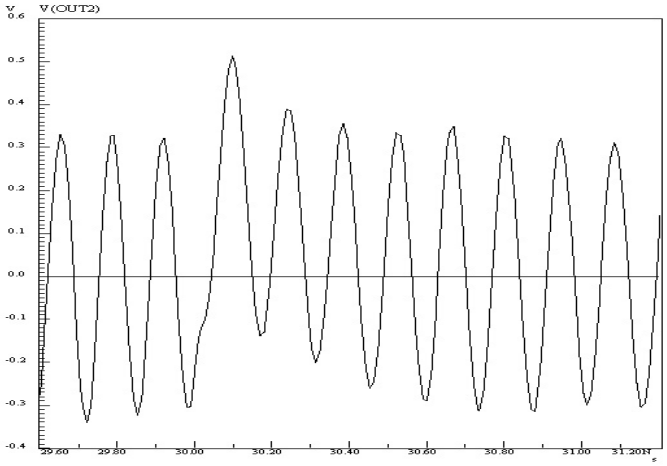


Figure 8.27. Frequency shift from 7656 MHz to 7128 MHz occurs in less than 2 ns.

8.4 Frequency Conversion Unit for Digital Period Synthesizer

Conventional frequency synthesizers based on phase-locked loops suffer from many limitations, such as a limited tuning range, limited settling time, die area and power trade-offs, and poor reconfigurability. These issues are caused by the PLL operating restrictions and by poor oscillator characteristics. Most synthesizer researchers are well aware of these problems, and therefore completely new solutions are being explored. We have developed a wide-band digital frequency synthesizer that is based on digital period synthesis (DPS). The related invention has been filed [8.114], and the results of the first circuit implementation are reported in [8.115]. Our DPS prototype is able to cover a wide (over two-octave) frequency range. The range is limited at the lower end by the reference frequency, and at the higher end by the internal delays. A frequency conversion unit with divide-by-two, feed-through, multiply-by-two, and multiply-by-four functions was added to expand the overall frequency range of the implemented circuit. The frequency converter was added somewhat hastily after the frequency limits of the DPS unit had been found out. Furthermore, we knew that in future design cases we can derive quadrature outputs directly from the DPS unit. Therefore, in this first version we intentionally accepted the fundamental-tone leakage problem in multipliers caused by the lack of quadrature input signals.

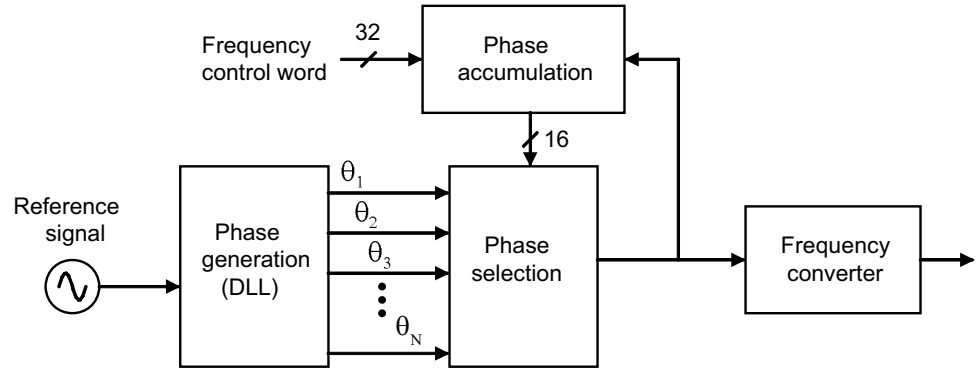


Figure 8.28. Conceptual structure of the direct period synthesizer.

The DPS output signal is generated from a set of sequential phases by selecting and combining them. The DPS consists of a phase generation unit, a phase selection unit, and a phase accumulation unit as depicted in Figure 8.28. The phase generation unit, which includes a delay-locked loop, forms N signals with the frequency f_{REF} and sequential phase. These signals (θ_1-θ_N) constitute the phase reference for the output signal generation. The phase selection unit

selects one of these reference phases at a time and combines them as an output signal. The phase accumulation unit controls the selection in such a way that the desired output periods are generated between successive output pulses. The frequency information for the accumulation unit is constituted from a digital frequency control word. The phase accumulator is clocked by the output signal instead of the reference signal to enable the digital period synthesizer to operate at frequencies higher than the input signal. The main timing requirement in the DPS originates from this feedback loop. To ensure the proper operation of the DPS, the accumulated phase selection data have to be ready prior to the next phase reference signal selection. As a result, the minimum output period that can be generated has to be longer than the accumulation delay (see [8.115] for details). This defines the maximum output frequency of the DPS. A delay of about 750 ps can be achieved with the 65-nm CMOS technology that was applied. This means that the maximum output frequency of around 1.5 GHz is possible for the DPS architecture, and furthermore some safety margin needs to be included. Conceptually, the DPS is just a frequency multiplier where a non-integer multiplication factor can be set with high precision. It has fine frequency resolution and a very short frequency settling time. Other benefits are its versatile structure, full compatibility with digital CMOS, and easy transfer as an independent IP block.

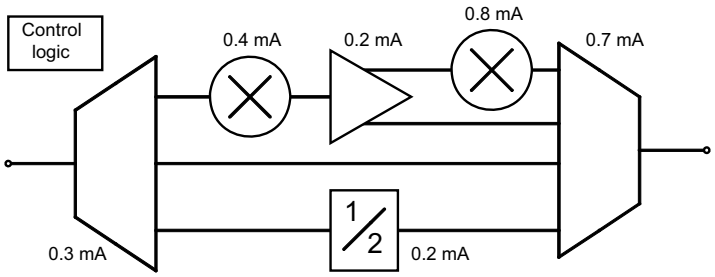


Figure 8.29. Structure of the frequency converter unit. The signals are differential, although they are drawn as single-ended. The simulated current consumptions of each block in active mode are shown.

The 200-MHz minimum output frequency of the DPS is set by the reference frequency and the maximum output frequency is about 1 GHz. The purpose of the frequency converter (FC) unit is to expand this frequency range. Since the DPS has an output range of over an octave, a continuous output frequency range will be available if binary-weighed (2^K, K=-1, 0, 1, 2,) frequency division and multiplication is used. The structure of the FC unit is depicted in Figure 8.29. It consists of a divide-by-two circuit, a feed-through mode, and multiply-by-two and multiply-by-four circuits. A de-multiplexing circuit (de-mux) divides the signal path into three parallel ones, one being active at a time, and correspondingly a multiplexing circuit (mux) connects the paths again. The de-mux is a common-source-type amplifier with separate selectable loads for each path. The mux circuit uses a common-gate-type configuration for each path and a common load. Furthermore, a buffer amplifier with P-MOSFETs in open-source configuration drives the external 50-Ohm level measurement environment. The divider is based on transmission-gate logic DFF, derived from the foundry-provided standard cell library and customized by us for pseudo-differential operation. According to simulations this circuit operates up to 7 GHz in the nominal process corner, so there is no speed-related reason to favor static SCL DFFs. Frequency multipliers are based on asymmetric source-coupled pairs [8.90]. The two multipliers are similar in structure, but have different device dimensions. The circuit schematic is shown in Figure 8.30. This circuit outperforms other multiplier candidates by being able to produce a less-distorted output signal with decent efficiency. This enables two multipliers to be chained. The aspect ratio S of the two transistors in an unbalanced pair sets the conversion gain, and the bandwidth is relatively independent of this choice. The conversion

gain saturates at high S values, so the design procedure is quite simple. This simplicity also indicates that this circuit is robust against process variations and other deficiencies.

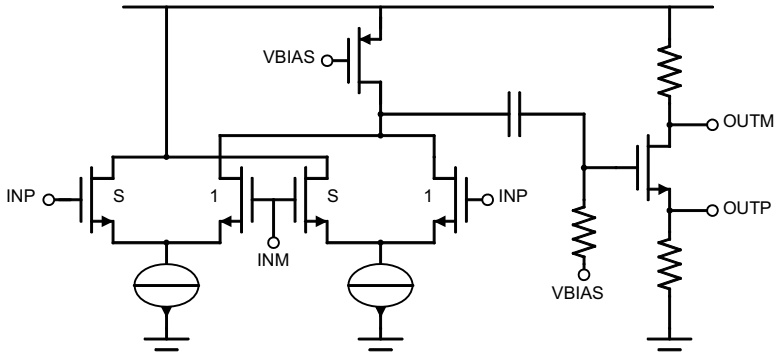


Figure 8.30. The multiply-by-two circuit consists of asymmetric source-coupled pairs, and a single-to-differential converter. The pair size ratio S is 7.

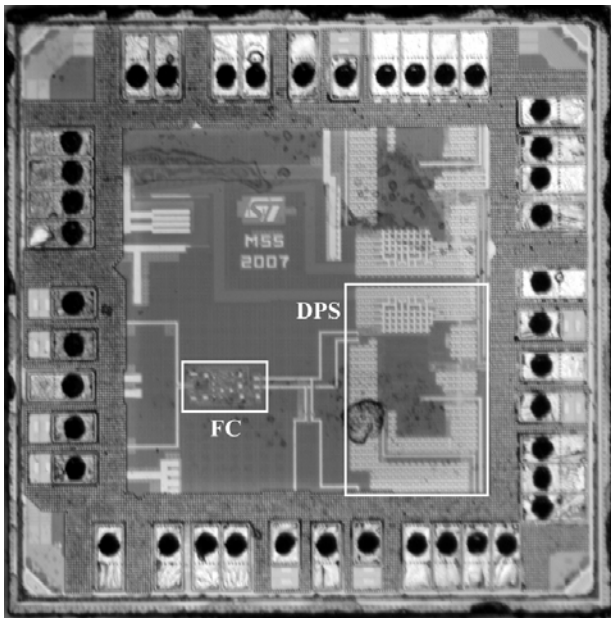


Figure 8.31. Microphotograph of the implemented circuit. The FC unit has dimensions of 130 x 60 μm. Altogether, the active area used by the synthesizer is 0.12 mm^2. The complete chip is about 1 x 1 mm.

The circuit was fabricated in a 65-nm CMOS process. A microphotograph of the die is shown in Figure 8.31. The decision to add a frequency converter to the circuit had two motivations. One was to expand the frequency range, just to demonstrate that it can be done, and the second motivation was an interest in noise performance. Noise issues are a topic about which simulations alone give insufficient information, and often some unknown or unexpected sources of noise reveal themselves in measurements. Figure 8.32 depicts the measured phase noise at different settings of the frequency conversion unit. The 640-MHz output frequency was arbitrarily selected at roughly the middle of the output range. Theoretically, the phase noise of the signal scales in binary-weighed frequency conversion with a 6-dB factor. Table 8.2 compares the measured values to the theoretical ones. We observe that the frequency converter operates well, and the impairment of the phase noise is small. Actually, the measurement accuracy is of the same order as the impairments, so we may indeed just conclude that the amount of added noise is small.

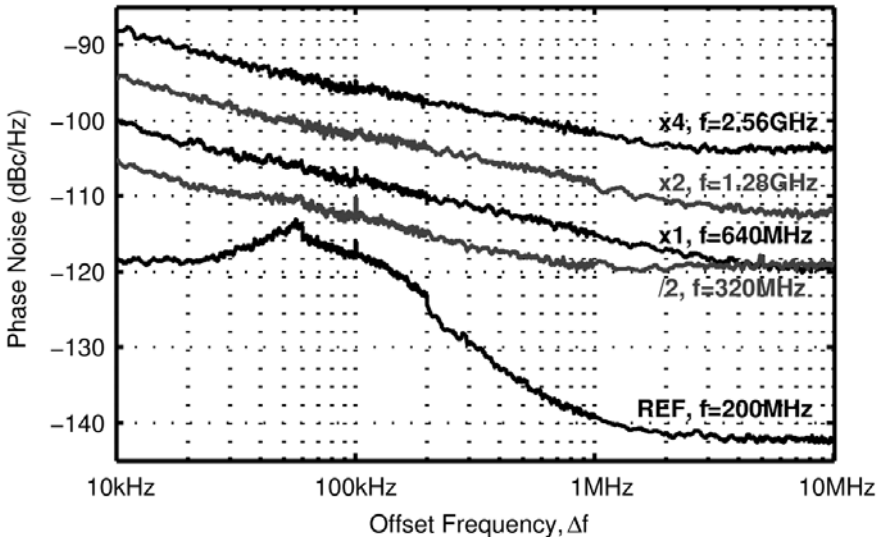


Figure 8.32. Measured phase noise at the FC output with different conversion settings.

Table 8.2. Phase noise impairment.

Mode	N/C [dBc/Hz] @ 100-kHz offset	Theoretical change	Impairment
Feed-through (x1)	-108	–	–
div-by-two (/2)	-113	-6 dB	1 dB
Multiply-by-two (x2)	-101	6 dB	1 dB
Multiply-by-four (x4)	-95	12 dB	1 dB

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9 Research Projects and Experimental Circuits

This chapter presents some research projects and experimental circuit development work. The emphasis is on describing the research background, the circuits that have been implemented, and the experimental results. Advisedly, no deeper analysis is presented here. The chapter begins with a presentation of a temperature-compensated GaAs MESFET VCO. Then experimentally-oriented work with a 0.8-µm BiCMOS process is presented. Section 9.3 presents development work on a cable-modem double-conversion receiver. Then oscillator design for a flip-chip multi-chip-module technology is described. The last section is devoted to UWB synthesizers.

9.1 Temperature Compensated GaAs MESFET VCO

In this project the target was to design a versatile temperature-compensated GaAs MESFET VCO. The primary frequency range was set to 1.6 – 1.7 GHz, but it was hoped that the same circuit could be used in other bands as well to allow wider commercialization. A further target was for this VCO that it could drive external mixers directly, and therefore the output power requirement was set to be as high as 10 dBm. The process that was applied was a 0.7-µm GaAs E/D-MESFET technology, which included both enhancement-type MESFETs (EFET) and depletion-type MESFETs (DFET). Both transistor types have the same f_t=17 GHz. The project was carried out in three phases. First, two oscillators were designed and measured. These worked well, but did not meet the main requirements as a result of an improper MESFET varactor model that was used. MESFET varactor-related issues were discussed in Section 6.2, and Figure 6.4 depicted the highly non-linear series resistance. In the second phase five oscillator variants, and a secondary version for each to ensure proper operation in an extreme process corner, were designed and measured on-wafer or by wire-bonding the chip to a printed circuit board. The best candidate out of these was encapsulated into a plastic SO-8 package. Here I will describe only the final packaged circuit in order to keep this section concise. These results were published in [9.1].

9.1.1 Circuit Description

The oscillator circuit is based on the single-ended common-gate Colpitts configuration. The circuit schematic is shown in Figure 9.1. The circuit has a partly external resonator for coarse frequency tuning. The monolithic 2-nH coil has a Q-value of only 6 at 2 GHz, and this dictates the quality factor of the overall resonator. We chose to use only a partly external resonator so as to avoid multi-oscillations and to enable measurements also to be taken without an external resonator. In a test circuit board a transmission line acting as a resonator is terminated with a capacitor, and the location of this capacitor defines the coarse frequency band. The circuit that was implemented operates in the 1 – 2 GHz range with different settings of the external inductance. The upper limit is set by the internal inductor and the inductance of the lead and the bond wire, altogether about 4 nH. The lower limit is not precise and the circuit oscillates at least at 0.5 GHz. However, as the buffer-amplifier is AC-coupled the output power remains low, and hence the circuit is not useful below 1 GHz. The fine-tuning of the oscillation frequency is performed with a MESFET varactor. The tuning range of the varactor with a three-volt tuning is 8.3:1, but it is only 1.8:1 in the low-loss region. In addition, the oscillator includes a temperature-compensation circuit. The VCO core current is slightly adjusted with a temperature-dependent bias voltage. A three-stage output buffer-amplifier is used to provide sufficient isolation and high output power. The common-drain buffer has high input impedance to prevent excessive loading of the oscillator. The amplifier itself consists of an actively loaded

common-source stage with a self-regulating DC operating point, and a common-source stage with an inductive load. The circuit utilizes two supply voltage rails and two ground rails to avoid unwanted instabilities caused by package lead inductances. The simulated current consumptions are: temperature compensation 11 mA, oscillator core 7 mA, and buffer-amplifier 78 mA.

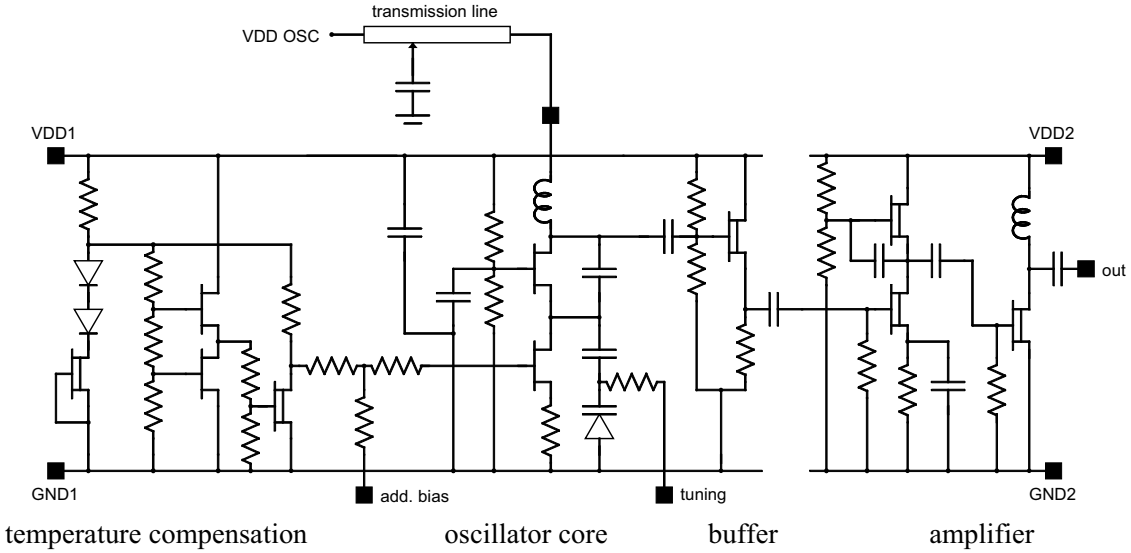


Figure 9.1. Schematic of the implemented circuit. Black boxes indicate bonding pads.

9.1.2 Temperature Compensation

The basic idea of temperature compensation is to apply a temperature-dependent biasing to the oscillator and hence vary the operating point according to the temperature. A small variation in the bias point of the oscillator causes a corresponding variation in the oscillation frequency. When properly designed, this variation cancels out the natural temperature variation of the oscillation frequency. Without any temperature stabilization the oscillation frequency variation is about 40 MHz within a temperature range -20 – +70 C. The change in the varactor capacitance causes ¾ of this, and the rest is due to the oscillator core. In the circuit the bias resistor of the core oscillator is replaced by a transistor acting as a tunable current sink, and a temperature-dependent bias voltage is connected to the gate of the transistor. Four evolution versions of the circuit generating a temperature-dependent voltage are shown in Figure 9.2. The first two circuits utilize DFETs, while the third one includes EFETs. All the circuits generate an output voltage with a linear temperature response. With a 3-V supply the output voltage variation in the temperature range of -20 – +70°C is less than 10 mV for the first circuit, less than 100 mV for the second case, and in the EFET case it exceeds 400 mV. In addition, with DFET-circuits only one design parameter, the ratio of the channel widths of the DFETs, is available, while in the EFET case the designer may also vary the bias point of the lower FET. This additional design parameter somewhat alleviates the design procedure for the desired characteristics. The current consumption is also slightly lower in the EFET case, although in our circuit the current consumption of the temperature compensation circuit is small compared to the amount of current consumed in the amplifier stages. The fourth circuit depicts an additional inverter used to change the slope of the output voltage. This type of temperature compensation scheme essentially increases the pushing (the sensitivity of the oscillation frequency to the supply voltage level). A simple bias arrangement was included to reduce the pushing figure. The temperature compensation circuit also has an additional input/output point (the pad with the label “add. bias” in Figure 9.1) that enables the post-tuning and testing of the operation of the temperature compensation circuit to be performed.

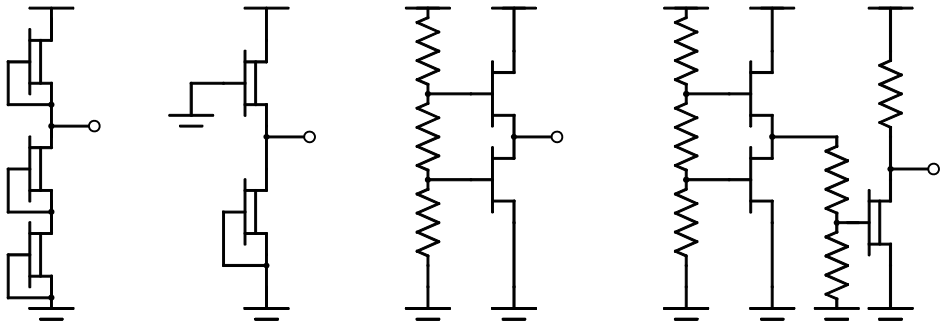


Figure 9.2. Evolution of temperature dependent voltage generator.

9.1.3 Measurement Results

The die photograph is presented in Figure 9.3. The layout is not very dense, because the size of the die, 1 x 2 mm, was fixed at the beginning of the project and therefore we were allowed to make a spacious layout. The packaged circuit was attached to a FR-4 type printed circuit board, and the placement of a 10-pF SMD capacitor with respect to the external microstrip resonator was set to be such that the oscillation frequency is close to 1600 MHz with a zero tuning voltage setting. The tuning characteristics of the circuit are shown in Figure 9.4 and the linear tuning range, specified in the design project, is shown in Figure 9.5. Figure 9.6 depicts a phase noise measurement carried out at Ylinen Electronics Inc. In Figure 9.7 the sensitivity of the oscillation frequency to temperature variation (-20 ... +70 °C) is plotted. One of the five oscillator variants had almost the same core as the packaged circuit but no temperature compensation circuit and it was used as a reference because it gives about the same performance characteristics as the VCO reported here. The frequency stability over the defined temperature range varied from 18 to 36 MHz depending on the tuning voltage for the uncompensated circuit. For the compensated circuit it was from 6 to 20 MHz. Finally, we used the possibility of tuning the bias voltage externally. A 0.3-V voltage with a 180-Ω source resistance was simply added to the bias node (Figure 9.1, label add. bias). With this post-tuning the frequency stability improved even more and it varied from 0 to 8 MHz. The performance characteristics of the final VCO are summarized in Table 9.1.

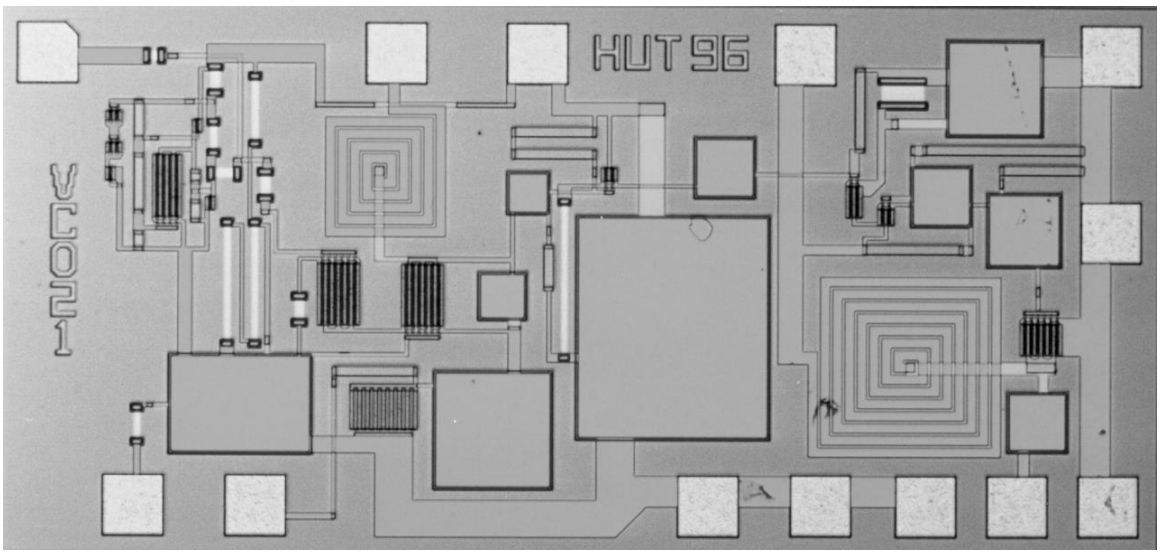


Figure 9.3. Microphotograph of the circuit.

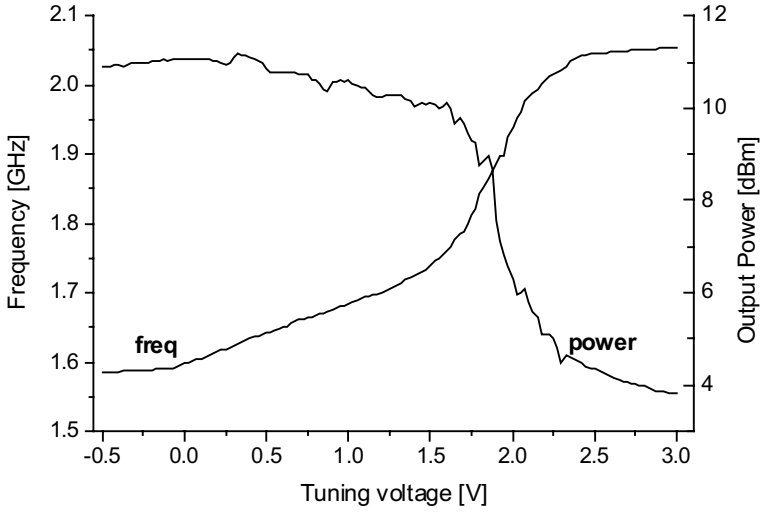


Figure 9.4. Overall VCO tuning characteristics.

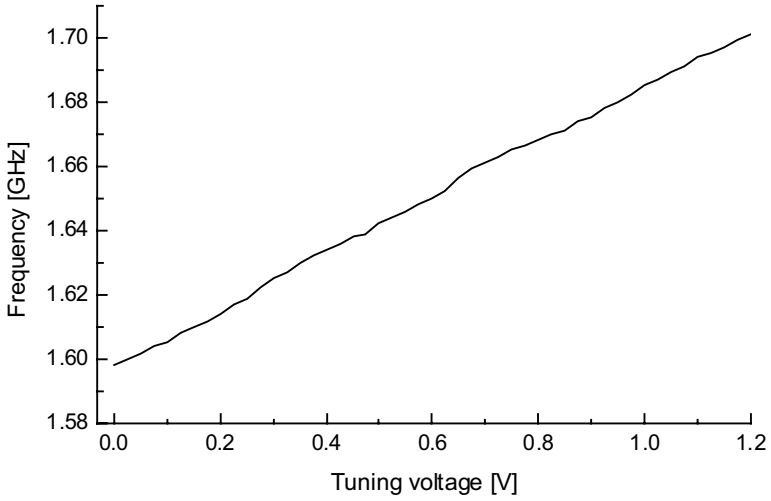


Figure 9.5. Linear tuning range.

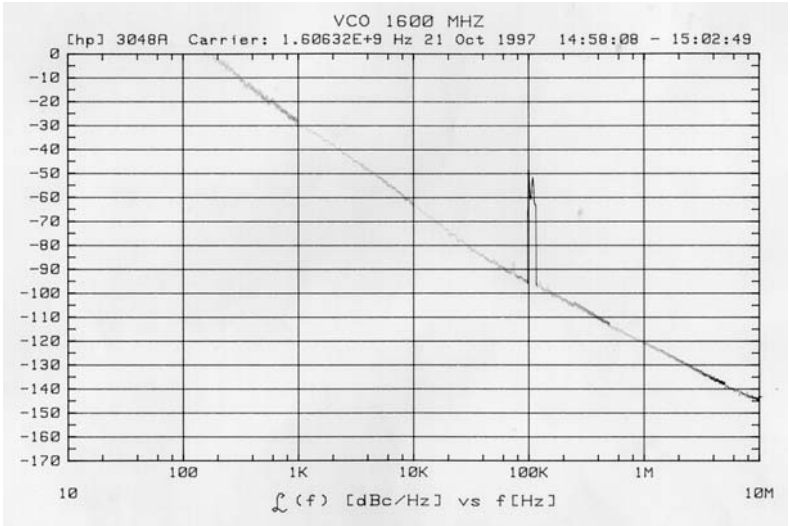


Figure 9.6. Phase noise measurement at 1606 MHz. The measurement system generates the spike at the 100-kHz offset.

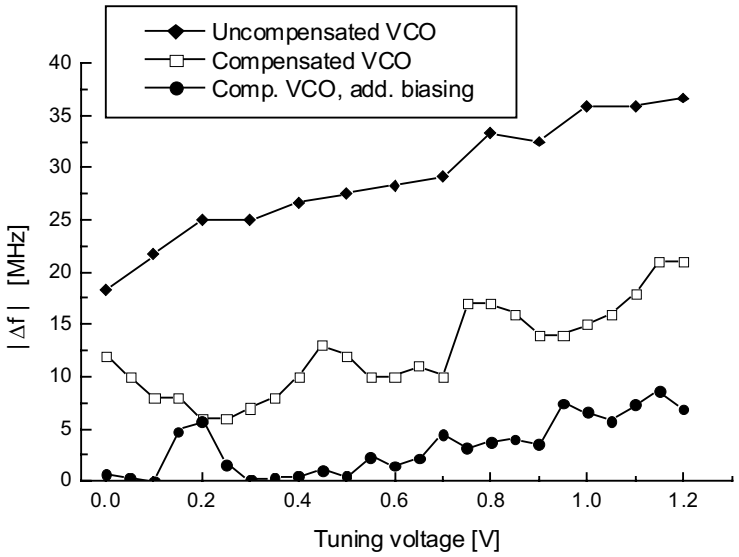


Figure 9.7. Measured oscillation frequency drift resulting from temperature variation. The temperature range is -20 °C…+ 70 °C.

Table 9.1. Performance summary.

Technology	0.7-μm E/D-MESFET
Linear tuning range	1600 – 1700 MHz
Output power	+ 10 dBm
Distortion (THD)	-21 dBc
Frequency stability vs. temp.	8 MHz
Output power stability vs. temp.	1.5 dB
Temperature range	-20 °C…+ 70 °C
Pulling (VSWR=1.67)	5 MHz
Pushing (Vdd ± 5%)	5 MHz
Phase noise @1 MHz	-120 dBc/Hz
Supply voltage	3.5 V
Current consumption	100 mA
Oscillator FOM	170

9.2 Circuit and Device Development with *VTTB8*

VTTB8 was a 0.8-μm BiCMOS process from the Technical Research Center of Finland (*VTT*) [9.2]. It was oriented towards research into semiconductor physics and manufacturing, but they did offer multi-project-wafer (MPW) runs once or twice a year. The MPW program was closed at the end of the year 2000, when the process had become very old-fashioned and the foundry infrastructure was focused on new fields, such as silicon MEMS devices. Actually, the process infrastructure was a joint effort of both *VTT* and *TKK*. Therefore, *TKK* was offered some free die area from the MPW runs. During 1997-2000 I participated in these activities by designing six test chips, which included altogether 38 oscillators, 21 monolithic test coils, 15 varactors, and 7 capacitors. Some of these experiments, though, had fabrication-related defects and therefore did not provide any results. In order to be able to understand the work done in proper perspective, a little discussion of the status and characteristics of the process is needed. Actually, I am not really complaining about the shortcomings of *VTTB8*. The fact that both the technology and the design kit needed special attention led to many activities. By working with these challenges I learnt a lot of practical engineering skills. However, from the academic point of view a huge amount of work was done that still resulted in just a few publications.

VTTB8 was a 0.8-μm gate length, double well, double poly, and double metal BiCMOS process. It included a polyemitter npn bipolar transistor with a 16-GHz cut-off frequency (f_t). The foundry provided parameters for the poly resistors and poly-poly capacitors, but no RF-dedicated models were available for any passive devices. The process did not include salicided poly-silicon, meaning that the gate resistance in the MOS transistors and in the corresponding MOS varactors was high, and therefore these devices had poor high-frequency properties. Both metal layers had quite a high sheet resistance. Therefore, the inductor Q-values remain low, typically about 3 at 2 GHz. Furthermore, the lower metal was close to the substrate, resulting in high parasitic capacitance. Therefore, the metal1-metal2 MIM capacitors had a C/C_{par} ratio as low as three. Since no RF-dedicated models for passives were available, I had to measure and model a large set of test devices. Eventually, I was able to establish an RF model library that enabled some RF VCOs to be designed successfully. Bipolar transistors were the key devices in the oscillator design. The foundry provided three sets of parameters. The first one was for a larger transistor with 1.2-μm wide emitter strips, and the second one was established in 1996. The third parameter set from a run in 1997 predicted some odd behavior, and therefore was not trustworthy. So the second model was the only somewhat reliable one, and yet it was fabricated in the old environment, since the actual fabrication plant was moved into a new building during 1997. Another issue worth mentioning here is that in the early phase the foundry personnel were not able to define what the sheet resistance of the second poly used for polysilicon resistors would be. Therefore, I decided not to use them so as to keep the unknown issues to a minimum. The current sources in the oscillator circuits therefore do not include emitter degeneration, and this increases the phase noise by some 5-10 dB. This was a mistake on my part. Current sources can withstand high levels of variation in absolute values of emitter degeneration resistors as long as the matching is good.

My work on the device and circuit development with *VTTB8* had three focus areas. The modeling of passive devices has been discussed in Chapters 5 and 6, and oscillators utilizing active tunable capacitors were described in Section 7.3. Therefore, here I will present only the cross-coupled transistor pair oscillators. Most of these circuits have been presented in [9.3].

9.2.1 Circuit Descriptions

In the early phase of this work MIM capacitor models were not yet available, and therefore circuit topologies based only on DC coupling were used. Furthermore, the circuits were measured on-wafer using probe heads with the ground-signal-ground-signal-ground (GSGSG) configuration. Therefore, only the supply voltage and tuning voltage were fed into the circuits, and the balanced RF signal was taken out. Four types of cross-coupled transistor pair (CCP) oscillators were implemented, and within two runs two types of resonators for the 2-GHz and the 4-GHz range were exploited. The 2-GHz resonator includes two 3.9-nH single-ended coils and two varactors consisting of eight BJT units. Correspondingly, the 4-GHz resonator has 1.4-nH coils and ten-unit varactors. The resonators are different in terms of the polarity of the varactor diodes. In the 4-GHz resonator the collectors and emitters of both npn-based varactors are connected together, while in the 2-GHz resonator the bases are connected together. The collector-emitter nodes have significantly larger parasitic capacitance and hence the capacitive tuning range is smaller. The circuits that were implemented are named according to the circuit structure and the type of the resonator. Accordingly, they are *CCP1_2G*, *CCP2_2G*, *CCP3_2G*, *CCP4_2G*, *CCP1_4G*, *CCP2_4G*, *CCP3_4G*, and *CCP4_4G*. The basic CCP schematics are shown in Figure 9.8, and as an example the complete schematic of *CCP3_2G* is shown in Figure 9.9. All the other circuits have similar bias and output arrangements. CCP1 is the basic cross-coupled pair. It has the bias setting $V_{CE}=V_{BE}$, and $V_{BC}=0V$. Therefore the oscillation amplitude is quite limited and the oscillator enters the voltage-limited region a little earlier than $V_{osc,pp}=V_{BE}$. CCP3 and CCP4 use source-followers to set the bias to $V_{CE}=2V_{BE}$ and therefore the oscillation amplitude is higher. CCP4 has a very simple layout since all the DC current is driven through the coils. This may be beneficial in some really high-frequency applications, but here the experimental results reveal that CCP4 is inferior to CCP3. CCP2 emerged from studies on how to reduce the parasitic capacitance presented by the negative conductance unit. I studied various ways of coupling the cascode transistor, used, for instance, in low-noise amplifiers to isolate the input and output nodes. CCP2 does indeed show some improvement in the higher-frequency circuit, but none at lower frequencies. I have also studied this circuit with other BJT technologies and it is generally not a good choice. Here it actually benefits from the high base resistance of the BJTs in this technology. In addition to these eight circuits, in the last available process run I exploited the results of device development. The two circuits that were implemented include MIM capacitors in the cross-coupling path, external biasing with the aid of PMOS transistors, and differential coils. Furthermore, these circuits included real optimized pn-junction varactors instead of npn-based devices. The circuits are named *diffVCO1* and *diffVCO2*, and they differ only in the structure of the coil. The coil strip widths are 20 μm and 40 μm, respectively. Figure 9.10 depicts the circuit schematic.

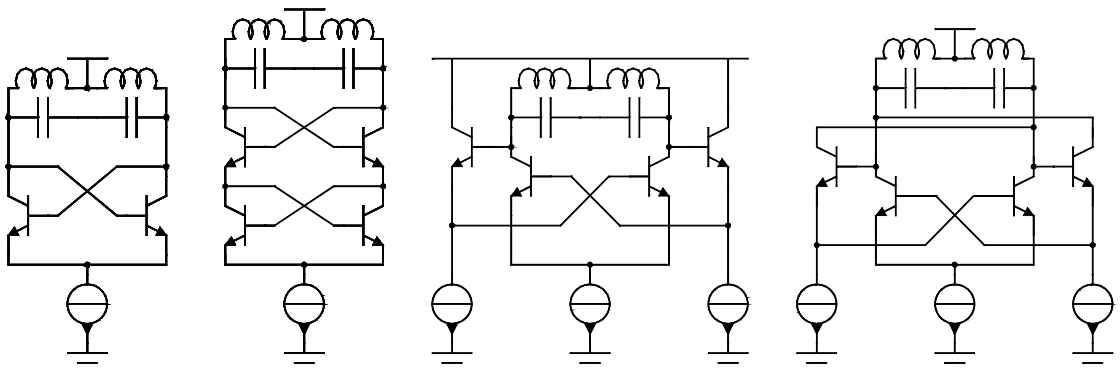


Figure 9.8. Structures of the CCP variants.

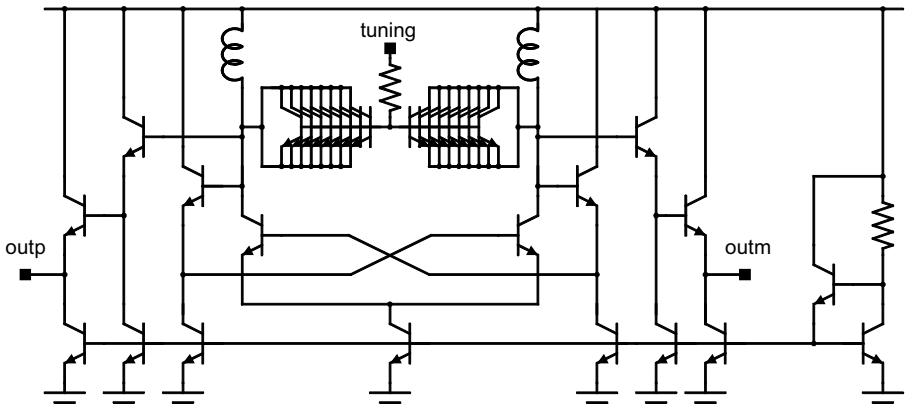


Figure 9.9. Schematic of the *CCP3_2G* circuit.

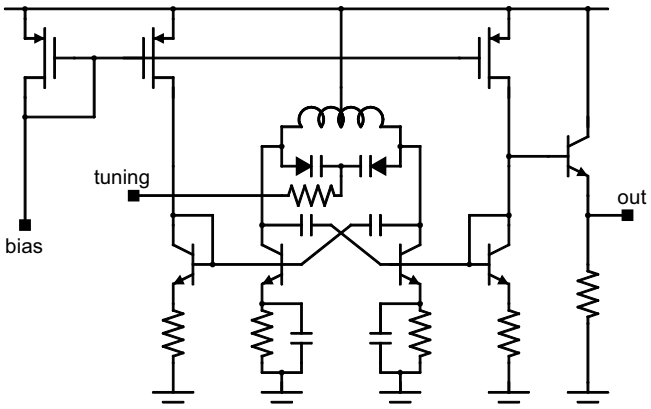


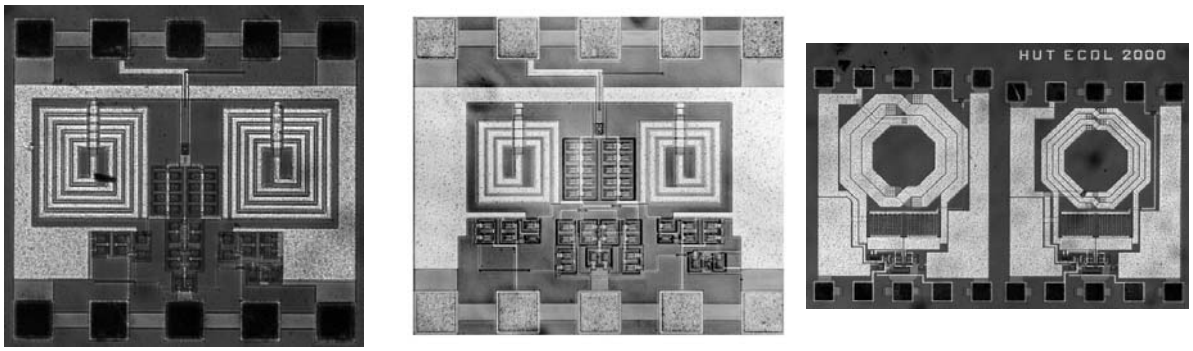
Figure 9.10. Schematic of the diffVCO circuits.

9.2.2 Measurement Results

The ten oscillator circuits were fabricated in three process runs. Examples of some oscillator layouts are shown in Figure 9.11 and one complete die in Figure 9.12. All the circuits are measured using two opposite GSGSG probe heads. Because of space limitations only a couple of measurement results will be depicted here as typical examples, but all the results are summarized in Table 9.2. Figure 9.13 shows a typical phase noise measurement result, here for *CCP3_2G*. Averaging in the measurement instrument (HP 4352B) was used to achieve a clean curve. Figure 9.14 depicts the oscillation frequency and phase noise at a 1-MHz offset over the tuning range for *diffVCO1*. Here no averaging for the phase noise measurement was used and therefore we observe large random deviation. Furthermore, here we see that the phase noise does not have a clear dependency on the tuning voltage. Table 9.2 includes a column for the oscillator core current. Since this cannot be measured directly it is estimated from the simulated values by scaling them with the ratio of the simulated and measured total current consumptions. The core current is then used for calculating the oscillator FOM. *DiffVCO1* and *DiffVCO2* had slightly different 2-kΩ and 4-kΩ external bias resistors that were chosen to achieve good performance.

The main research topic here was to learn how to design RF circuits with an experimental-level process that had only preliminary-level transistor models available, and even these were subject to model uncertainty and an unknown amount of process spread. Therefore, the circuit design targeted reliable operation, not optimum performance. Eight basic CCP oscillators were designed and measured successfully. Thereafter, by the carrying out of device development and

modeling for monolithic coils and pn-junction varactors, and after the gathering of some design experience, the later circuits, such as the *diffVCO1* circuit, actually show quite good performance, keeping in mind that it is implemented in a two-metal 0.8-µm BiCMOS process.



(a) (b) (c)

Figure 9.11. Microphotographs of (a) *CCP2_2G* (b) *CCP4_4G* (c) *DiffVCO1* and *DiffVCO2.*

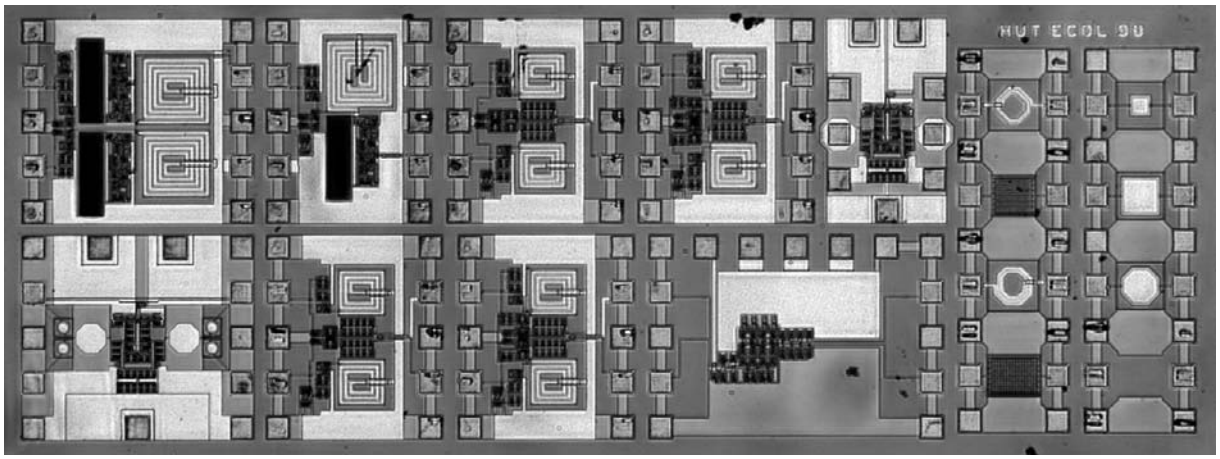


Figure 9.12. Microphotograph of a complete die including four CCP-oscillators, two Miller-capacitor oscillators, two active inductance filters, a frequency divider, two test coils, two varactors, and three MIM capacitors. The pad pitch is 150 µm and GSGSG probe heads were used for measuring these circuits.

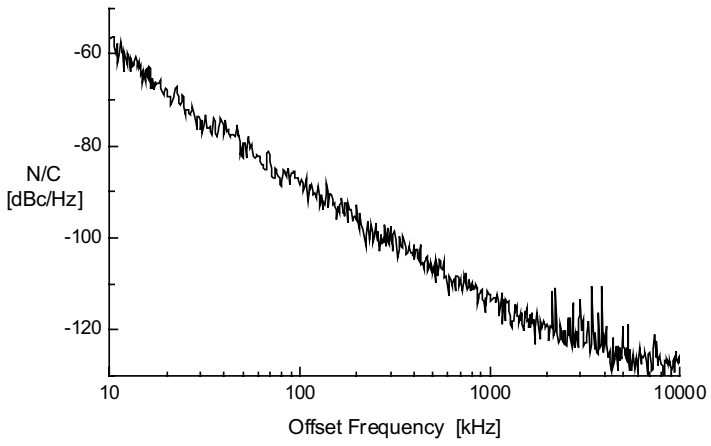


Figure 9.13. Phase noise measurement result for *CCP3_2G*.

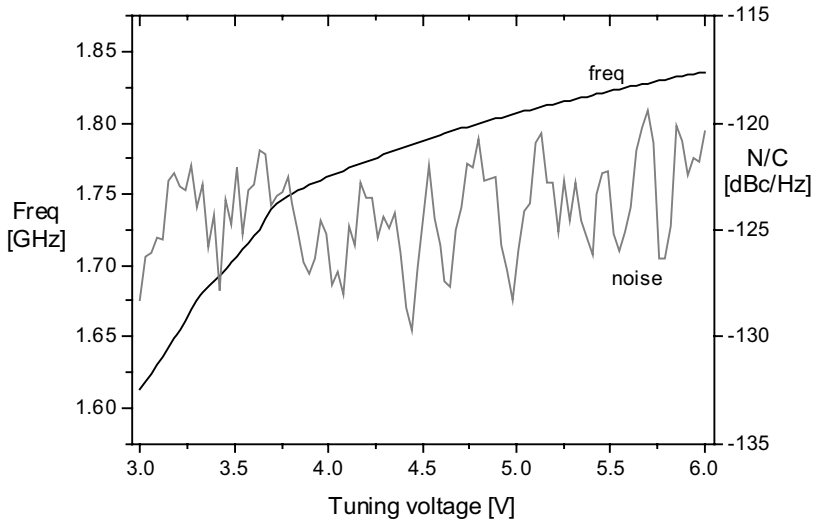


Figure 9.14. Oscillation frequency and phase noise variation over tuning for *diffVCO1*.

Table 9.2. Measured performance summary for CCP oscillators implemented with *VTTB8*. The supply voltage is 3 V and the tuning voltage range is 3 V.

Circuit	$I_{DC,total}$ [mA]	$I_{DC,core}$ [mA]	Center freq [MHz]	Tuning range	N/C@1MHz [dBc/Hz]	FOM
CCP1_2G	14	3.1	2100	5 %	-103	160
CCP2_2G	14	3.1	2740	5 %	-106	165
CCP3_2G	19	8.8	2440	5 %	-112	166
CCP4_2G	19	8.8	2210	4 %	-106	159
CCP1_4G	5	1.2	4330	9 %	-93	160
CCP2_4G	5	1.2	5050	9 %	-97	166
CCP3_4G	8	3.9	4470	7 %	-95	157
CCP4_4G	8	3.9	4410	5 %	-88	150
diffVCO1	15	11	1730	13 %	-123	173
diffVCO2	11	8.3	2260	9 %	-117	170

center frequency = (freq,max + freq,min)/2 tuning range= (freq,max- freq,min)/center freq

9.3 Cable-Modem RF Tuner

In this project the target was to design prototype circuits for a cable-modem RF tuner. These cable modems are used for data transfer in fixed coaxial-cable TV networks. Consumers use these to gain high-speed internet access. The RF tuner block diagram and frequency plan are depicted in Figure 9.15. The tuner is based on the double-conversion receiver architecture. The input signal is first upconverted into a fixed intermediate frequency, here 1575 MHz, and then after filtering downconverted into 36 MHz in European systems or into 44 MHz in U.S. systems. This receiver architecture particularly relieves the requirements for the LO generation. A smaller relative tuning range is enough and the LO leakage is not an issue. Chronologically, we started by designing the downconverter unit, and after successful implementation the work continued with the design of the upconverter unit. Therefore, we follow the same order here. There were altogether five process runs. The first two were for the downconverter development, although actually between these two runs we had an extra run where a frequency divider was re-fabricated, and some test devices and oscillators were added there too. The last two runs were dedicated to the upconverter. Within these five process runs we implemented altogether four downconverters, two upconverters, 14 VCOs, nine varactor test devices, and ten inductor test devices. The plan was to use an external commercially available dual-PLL for the VCO tuning, and therefore just prescalers were implemented in these designs. The decision was made to continue this project on an annual basis, and therefore we did not target full integration from the beginning, and also the passive test devices were just included to support the oscillator design, not really to develop better device structures. In this project we used a 0.9-μm SiGe bipolar process from *ATMEL* (previously *TEMIC*). Actually, we started to use this technology by first designing some low-noise amplifiers for the UMTS system [9.4]. The process – see e.g. [9.5],[9.6] – offered npn-transistors with a 50-GHz f_t, three metal layers (two layers in the first three runs), three types of resistors, inductors with a typical Q_{2GHz}=16, and metal-1 polysilicon capacitors with Q_{2GHz}=25 and C/C_{par}=37. The actual converter circuits were encapsulated into dual-in-line SSO36 packages, and the test circuits and devices were measured on-wafer.

This section consists of four subsections. First, four downconverter implementations are briefly introduced, and then the two upconverter circuits. In the third subsection the best downconverter and upconverter units are connected with filters to establish an RF tuner demonstrator. In the last subsection we take a closer look at the implemented oscillators.

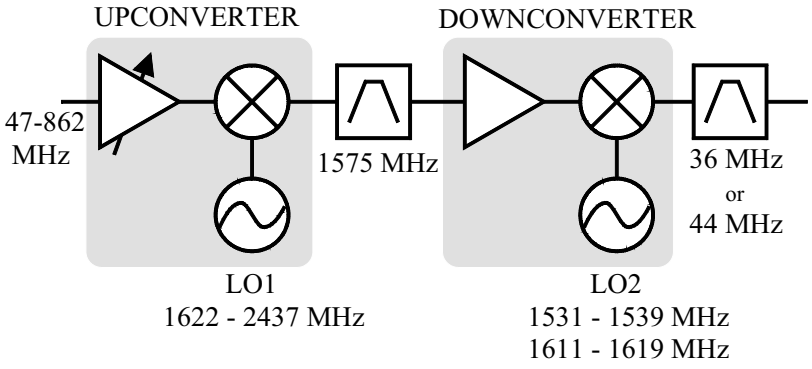


Figure 9.15. Double-conversion receiver architecture for cable-modem RF tuner.

9.3.1 Downconverter Units

The basic structure of the downconverter units is based on the Hartley image-reject architecture. A specific research topic here was how to implement the image selection. The

idea was to implement a circuit that is able to select whether the downconversion suppresses the input frequencies above or below the LO frequency. In constant-carrier RF applications we are able to select whether the LO frequency will lie below or above the signal frequency, and correspondingly, we can alter the image frequency. The system is able to switch the mode in the case of a very strong image, thus improving the quality of the downconverted signal. The signal phasing can be altered either in the IF segment or in the LO segment. These alternatives are depicted in Figure 9.16. The two corresponding circuit implementations are called *DwCon1* and *DwCon2*. Both circuits have similar building blocks; just the image-selection method is different. In *DwCon1* differential-pair type IF-amplifiers are set on or off, and in *DwCon2* a current-steering circuit is applied in the LO buffers to select the phasing of the LO signal. In the signal path the low-noise amplifier is a fully differential one-stage amplifier with cascode transistors in order to improve the isolation and minimize the Miller effect. A common emitter topology with inductive emitter degeneration is used for noise and input impedance matching. The mixers are conventional Gilbert cell mixers with resistive emitter degeneration for improving linearity. A three-stage poly-phase filter is used for signal combining. The IF-amplifier in these first circuits was simply two succeeding differential stages, and emitter followers were used as output buffers to drive the external SAW filter.

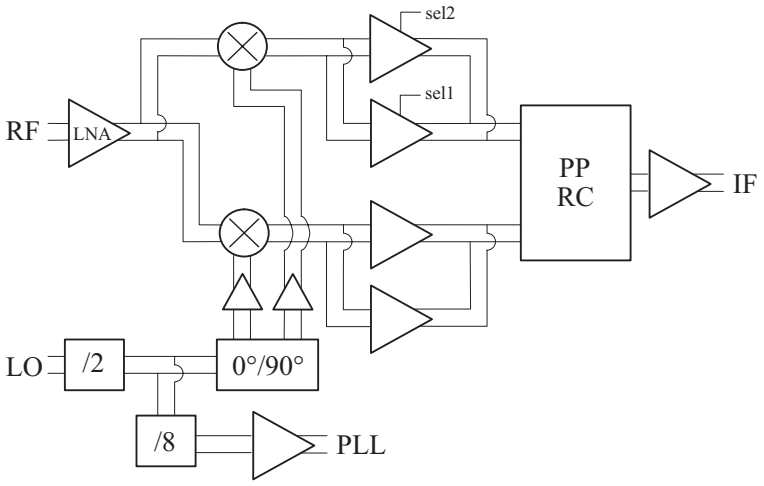


Figure 9.16. Block diagram of *DwCon1*. In *DwCon2* the image selection is performed in the LO buffers and the amplifiers between the mixers and PP filter are omitted.

In the measurements of these first circuits we found out that the frequency divider chain was not operating fast enough, and therefore the circuits were measured at a 750-MHz input frequency. The main results are summarized in Table 9.3. More details on these circuits can be found in [9.7]. We learnt that the image-selection functionality worked correctly in both cases, and since it is easier to implement it in the LO segment, that approach was selected for the next circuits. The frequency divider chain was completely redesigned and we also got a parasitic capacitance extraction tool that alleviated the design procedure. The IF amplifiers were also redesigned and, in particular, we developed a new type of output buffer to drive the SAW filter with better linearity and power efficiency [9.8],[9.9]. The new circuits are called *DwCon3* and *DwCon4*. They differ only in the type of oscillator and IF amplifier structure. The IF amplifier in *DwCon3* consists of two consecutive differential stages with feedback from the second stage back to the first one. This zero-pole cancellation scheme increases the bandwidth without sacrificing gain or linearity. The IF amplifier in *DwCon4* is a single-stage differential pair with cascode transistors. The main measurement results are summarized in Table 9.3, and a die photograph of *DwCon4* is shown in Figure 9.17. *DwCon4* had a sufficiently good performance, that we were able to proceed to the design of the upconverter unit. *DwCon4* was reported in [9.10].

Table 9.3. Measured results of the downconverter units.

	DwCon1 RF_{in}=750MHz	*DwCon2* RF_{in}=750MHz	*DwCon3* RF_{in}=1575MHz	*DwCon4* RF_{in}=1575MHz
Gain [dB]	46	52	43	44
IRR [dB]	40	46	45	40
NF_{SSB} [dB]	6.1	6.0	4.6	4.6
OIP3 [dBm]	22	24	18	20
I_{DC} [mA]	90	87	54	52

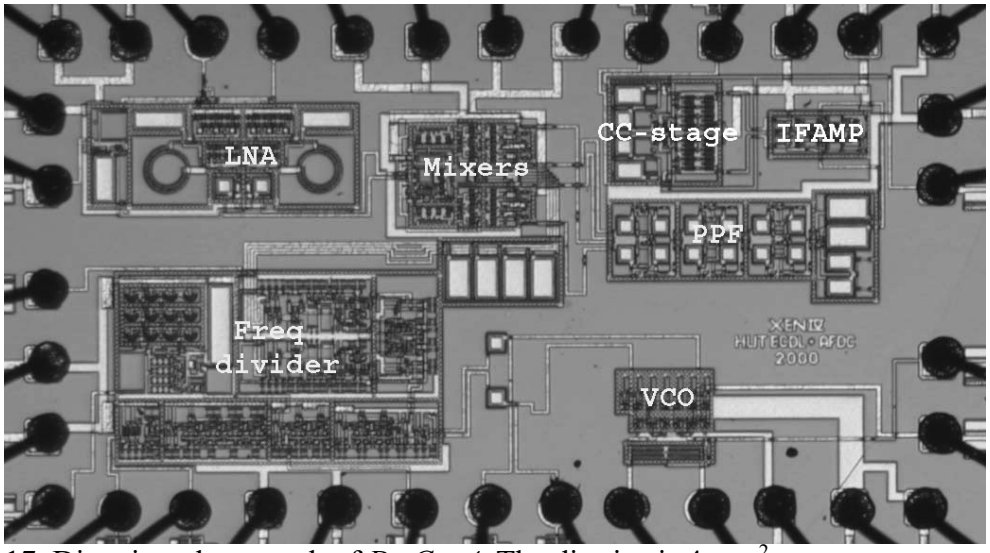


Figure 9.17. Die microphotograph of *DwCon4*. The die size is 4 mm^2.

9.3.2 Upconverter Units

Two upconverters were designed and implemented in two consecutive process runs. Here they are called *UpCon1* and *UpCon2*. They consist of a broadband low-noise amplifier (LNA), an upconverting mixer, and LO circuitry. The second one resembled the first one, and was just an improved version of it. The major improvements in the signal path were the inclusion of gain tuning into the LNA and better output matching. The first circuit was reported in [9.11], and since they are indeed quite similar I will just describe the latter one here. It was published in [9.12], [9.13]. The block diagram of *UpCon2* is depicted in Figure 9.18. The variable-gain low-noise amplifier (VGLNA) is a resistively matched balanced single-stage amplifier. It is depicted on the left in Figure 9.19. By using resistive matching, we were able to meet the required gain and noise figure while maintaining good impedance matching over the entire input band. The linearity is improved with small emitter degeneration resistors, unfortunately with a slight penalty as regarding the noise figure. Gain tuning is achieved by using the current-steering approach. Part of the signal is fed to the supply rail instead of the load resistors by altering the biasing of the current-steering transistors. The current-steering scheme does not alter the operation of the actual amplifying transistors. Thus the impedance matching and input-referred linearity remain constant. The mixer is a traditional double-balanced Gilbert-cell mixer with resistive emitter degeneration in order to improve the linearity. The mixer has an open-collector output to avoid power-hungry output buffers that might limit the linearity of the system. The mixer is depicted on the right in Figure 9.19. Here good output matching is essential for maintaining the correct filter response. The output impedance matching of the upconverter is achieved with a transformer, parallel inductors and series capacitors. The transformer is also needed to perform the differential-to-single-ended conversion required by

the first IF filter. The transformer is a transmission line step-up transformer (TLT) with a 1:4 impedance ratio. The output matching of the first circuit was inadequate, and that motivated us to develop a detailed equivalent circuit model for the transmission line transformer [9.14]. In *UpCon2* a good output matching of -20 dB at 1575 MHz was achieved with the aid of that model. Figure 9.20 depicts the die microphotograph of *UpCon2*, and the measured results are summarized in Table 9.4.

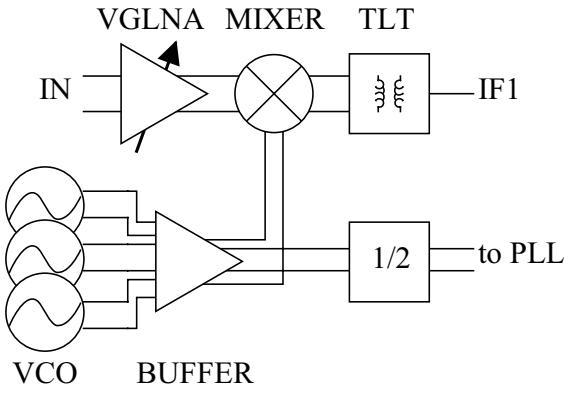


Figure 9.18. Structure of *UpCon2*.

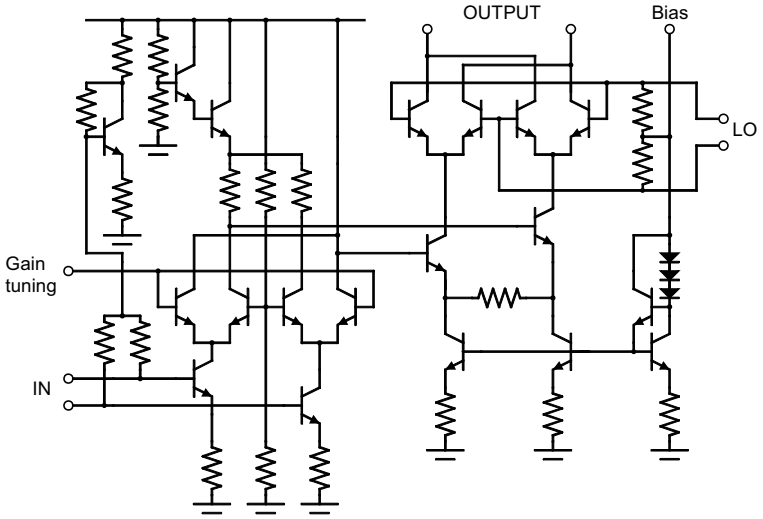


Figure 9.19. VGLNA on the left and the mixer on the right.

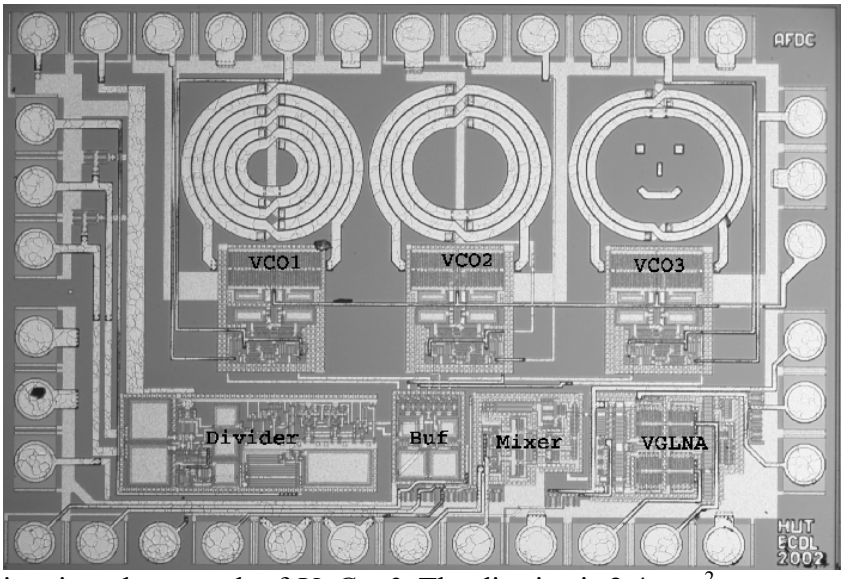


Figure 9.20. Die microphotograph of *UpCon2*. The die size is 2.4 mm^2.

Table 9.4. Measured results of the upconverter units.

	UpCon1	*UpCon2*
Input band [MHz]	47 – 862	
Output frequency [MHz]	1575	
Supply voltage [V]	5	
Current consumption [mA]	28	33
Gain [dB]	25 … 22	24 … 22
Noise figure [dB]	6.9 … 7.2	6.7 … 7.7
Linearity OIP3 [dBm]	15	17 … 15
Input matching [dB]	< -10 dB	-23 … -14
Output matching at 1575 MHz [dB]	-10	-20

9.3.3 RF Tuner Demonstrator

The upconverter circuit *UpCon2* and the downconverter circuit *DwCon4* were combined with SAW filters to establish an RF tuner demonstrator [9.15],[9.16]. The structure is depicted in Figure 9.21. An additional 10-dB attenuator was used since originally the downconverter had been designed for filters with a higher loss, and consequently the downconverter now has too high a gain. Figure 9.22 depicts the gain compression in the high-gain and low-gain modes. The gain tuning is sufficient and the tuner remains in a non-compressed mode with a 4-dB margin (2.5 dB is often required). The gain and noise figure over the defined input band are shown in Figure 9.23. The measurement results are summarized in Table 9.5.

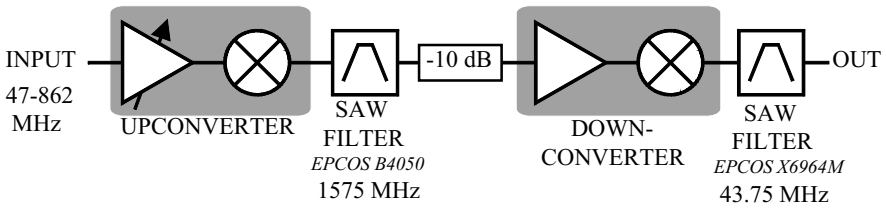


Figure 9.21. Structure of the RF tuner demonstrator.

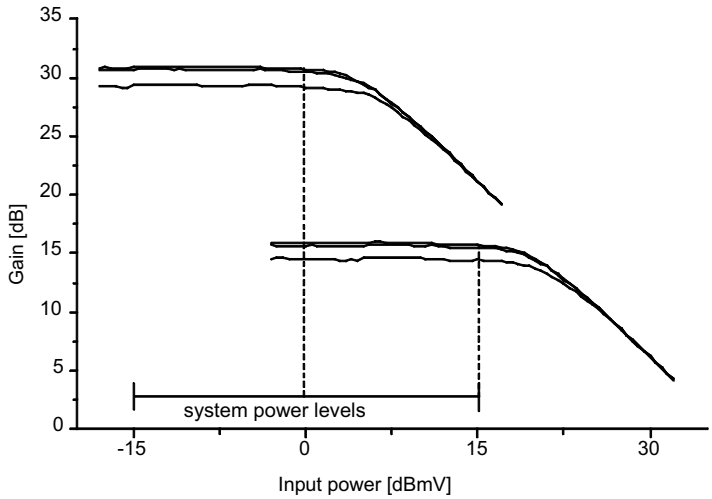


Figure 9.22. Measured gain compression for the tuner in the high-gain and 15-dB reduced low-gain modes. The three curves correspond to the frequencies 47 MHz, 450 MHz, and 862 MHz.
Unit dBmV converts into dBm in a 50-Ω system with: N dBmV = (N-47) dBm.

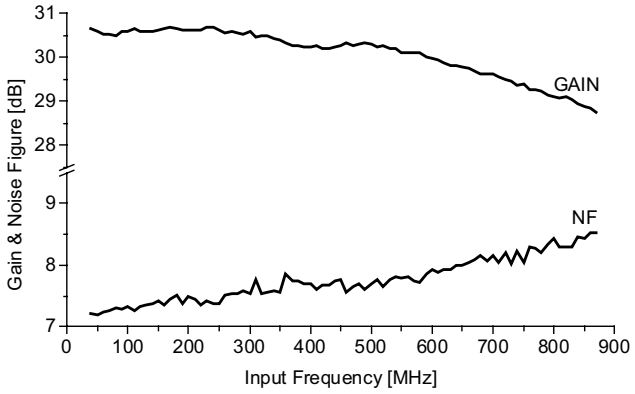


Figure 9.23. Gain and noise figure over the defined input band in the high-gain mode.

Table 9.5. Characteristics of the RF tuner demonstrator.

Input band	47 – 862 MHz
Output center frequency	43.75 MHz
Supply voltage	5 V
Current consumption	101 mA
Gain	30±1 dB
Noise figure	< 8.5 dB
Power levels (+margin)	-15 – 15 dBmV (4dB)
Image rejection	70 dBc
LO1 leakage to input	-45 dBm
Input matching	< -12 dB

9.3.4 Oscillator Implementations

The double-conversion receiver architecture that was selected sets quite different challenges for the design of the two LO signal sources. In the upconverter the main target is a wide tuning range with a sufficiently low phase noise. It turned out that this cannot be met with a single LC oscillator, and the unfortunate remedy is to use a set of parallel oscillators. In the downconverter we use the divide-by-four quadrature signal generation technique, and therefore the oscillators are in the 6-GHz range. The tuning range requirement is modest, but the frequency range itself sets demands for the accurate modeling of all the reactive elements. Because of these challenges, on a practical level the oscillator design in this project was actually very much struggling with the varactor and inductor models. Two types of pn-junctions were available for use as varactors. P^+-diffusion in a collector-well type diode, used for electro-static discharge (ESD) protection, has a smaller loss and smaller tuning range, while the base-emitter junction has a higher tuning range, but unfortunately also a higher loss as a result of the polysilicon layer that is used for the base formation. Therefore, this ESD diode was used in the 6-GHz oscillators, while base-emitter junction diodes were exploited in the 2-GHz oscillators to achieve a wider tuning range. Neither of these devices had an actual RF varactor model. Therefore, some model tweaking was needed. Eventually, after gathering experience of the process and by fabricating some test devices (summarized in Table 6.3) we got reasonably good results. The remaining issues that were actually unsolved at the end of our work with this process were process spread and the high leakage currents observed in some samples. In the case of the inductors we also met challenges. At the beginning of the project the foundry provided just some discrete-size devices, but later a scalable model was provided.

Then for the last two process runs the technology was improved by introducing a third interconnection metal layer. This improved the characteristics of the monolithic coils, but once again required new studies on inductor modeling, and the foundry-provided models were of preliminary status. Furthermore, all the devices supported by the foundry were single-ended, and this led me to design balanced structures with the aid of an EM-simulator. I "calibrated" the EM simulator by comparing the simulation results with the data provided by the foundry. Some discrepancies remained, regardless of what I tried. By reverse-engineering the foundry-provided scalable inductor model, I was eventually able to find the reason for these discrepancies. The scalable model provided by the foundry included an additional parameter that was used for presenting a pre-estimated length of the feed line the end user will draw into the layout. Unfortunately, this feature was completely undocumented and since I did take these feed lines into account myself, this resulted in some deviation between the simulations and measurements, and also caused problems for the calibration of the EM simulations. After solving these problems I was eventually able to design balanced coils with good accuracy.

Within the five process runs 14 oscillators altogether were designed and measured. The first nine were for the 6-GHz operation, and they were based on a very similar cross-coupled pair. The differences were mainly in the structure of the resonator. It would become slightly complex and messy story if they were all examined here. Therefore just four oscillators are presented and here they are called *VCO6G1* … *VCO6G4*. For the 2-GHz operation four oscillators were implemented in the fourth run and they are called *DualVCO1* … *DualVCO4*. In the last run a unit with three parallel oscillators was implemented and it is called *TripleVCO*. The 6-GHz bonding-wire VCO (*VCO6G4*) was published in [9.10], *DualVCO1* was published in [9.17], and *TripleVCO* was dealt with in [9.12], [9.13].

6-GHz Oscillators

These oscillators are all based on the CCP3-type negative conductance. This selection was made to avoid the use of low-quality metal-1 polysilicon capacitors. The oscillator schematic is shown in Figure 9.24 and a microphotograph of the first circuit is shown in Figure 9.25. The first circuit included two 1.8-nH inductors and the varactors were two parallel units of ESD diodes, so the area parameter was two. There was no scalable model for these diodes and a single unit was actually quite large. In the second run, which was the test run that was used mainly to test the corrected frequency divider, I tried to scale the ESD diode with a simple linear scaling, and the varactor area was 1.5 for *VCO6G2*. This linear scaling appeared to be insufficient, indicating that both area and perimeter factors do count. Here we also tried a lower supply of three volts, which makes the comparison here slightly unclear. In the third run *VCO6G3* included monolithic coils and the varactor areas were 1.95. In *VCO6G4* I tested the use of bonding wire inductors. The corresponding bonding wires are depicted in Figure 5.24. For this circuit the varactor areas were 3½. The measured results for these circuits are summarized in Table 9.6.

Table 9.6. Measured results for the 6-GHz oscillators.

Circuit	Supply [V]	$I_{DC,osc\ core}$ [mA]	Freq range [MHz]	Tuning range	N/C@1MHz [dBc/Hz]	FOM
VCO6G1	5	4.0	5470 – 6340	15 %	-88*	150
VCO6G2	3	2.6	6960 – 7630	9 %	-102	170
VCO6G3	5	2.6	5090 – 5670	11 %	-106	170
VCO6G4	5	2.6	5800 – 6620	13 %	-105	170

* Measured with spectrum analyzer

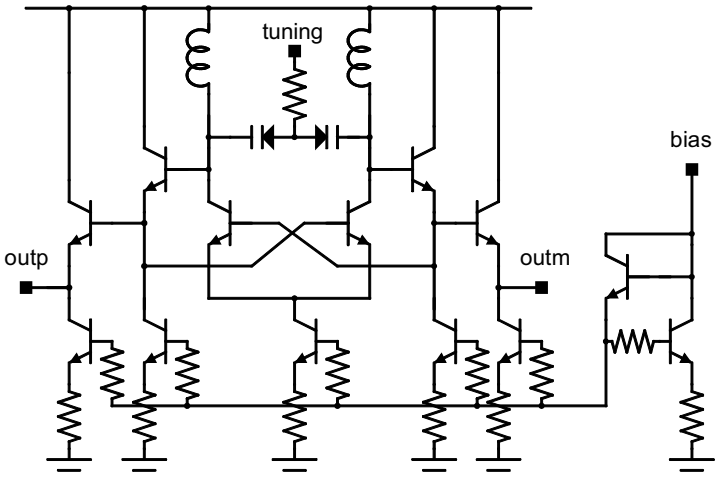


Figure 9.24. Oscillator schematic for the 6-GHz oscillators.

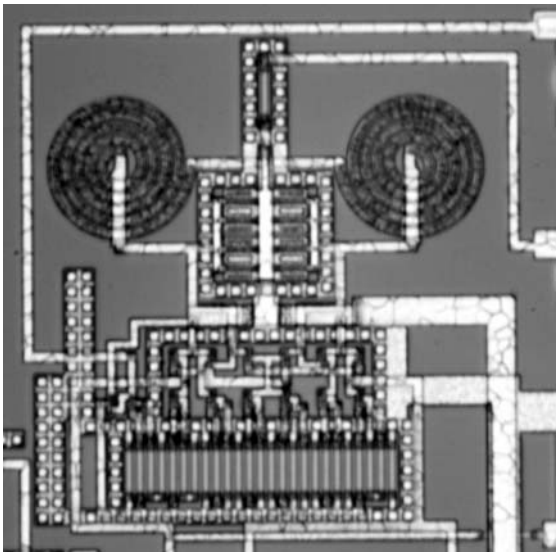


Figure 9.25. Microphotograph of *VCO6G1*.

Dual VCOs

The main design challenge for the LO generator used in the upconverter was to cover the wide frequency range of 1622 – 2437 MHz. Inherently wide-tuning-range first order oscillators, such as ring oscillators, suffer from too high a phase noise for this application. An LC oscillator is mandatory to meet the phase noise requirements. Unfortunately, these suffer from a very limited tuning range. The tuning range can be increased by means of exotic techniques such as applying an active inductance or active tunable capacitor. However, VCOs based on these techniques have high phase noise. In the MOS technology it is possible to use switched capacitors or inductors, but in a pure HBT technology no switch with adequate performance is available. Furthermore, it is possible to enhance the tuning range of a varactor-tuned VCO by forward-biasing the varactor. A penalty of about 10 dB in phase noise is observed in such cases, and performance predictability is poor. The simulations do not agree well with the real performance because of the inadequate varactor models in the forward-bias region. After these considerations the final candidate is an oscillator bank: several VCOs with different frequency ranges are in parallel and one of these is active at any one time. Four [9.18] or as many as eight [9.19] parallel oscillators have been used. The number of VCOs has a major impact on the total die area and therefore they should be kept to a minimum. As large a varactor as possible is required for the largest tuning range. However, a large varactor implies a very small inductance

value, and correspondingly, a low oscillation amplitude, poor phase noise, and high current consumption. A large bias current requires large active devices with large parasitic capacitance, and hence, the improvement in the tuning range will saturate. Accordingly, an optimum for the size of the varactor exists, where the tuning range is still large, but sufficient phase noise characteristics are achieved with reasonable current consumption.

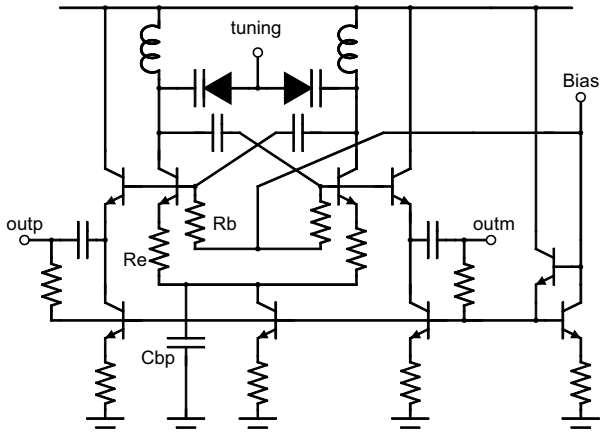


Figure 9.26. Schematic for *DualVCO1* and *2*.

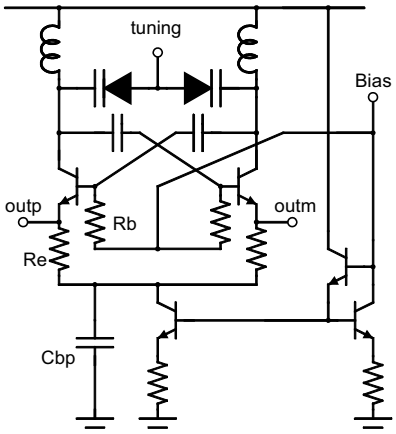


Figure 9.27. Schematic for *DualVCO3* and *4*.

For these 2-GHz oscillators I decided to apply the RC-biasing scheme, since these oscillators can tolerate the mediocre characteristics of the decoupling capacitors. The two circuit structures that were used are depicted in Figures 9.26 and 9.27. It appears that the DC-decoupling of the cross-coupled pair is beneficial, since the oscillation swing may forward-bias the base-collector diode for a period of an oscillation cycle in a direct-coupled pair, resulting in damping and the generation of additional noise. The phase noise vs. the bias point is shown in Figure 9.28. In this simulation a linear resonator with Q=10 is used. A strongly reverse-biased base-collector junction is better than just using a direct-coupled pair (V_{BC}=-V_{BE}) or coupling through voltage followers (V_{BC}=-2 V_{BE}). This improvement in the phase noise level is stronger at small offsets, but it is still observable even at large offsets. The resistor Rb used for biasing the bases does introduce additional uncorrelated noise, but simulations verify that the contribution to the total noise is negligible. Small emitter-degeneration resistors Re are used in these oscillators to suppress the harmonics and to reduce the up-converted noise. Even-mode distortion in the resonator voltage swing is smaller, resulting in a lower phase noise caused by the varactor nonlinearities. The emitter resistors add thermal noise and actually, although the phase noise is reduced at small offsets, it is slightly increased at large offset frequencies. In these designs the change from a positive impact to a negative one occurs at around 100 kHz. In this project a specific phase noise requirement was defined for a 10-kHz offset, and I therefore considered these techniques to reduce the phase noise at small offsets. The base resistances of the active devices are a significant source of noise in these types of circuits. Large devices can be used to reduce, but with the penalty of larger parasitics. Thus, again we have the phase noise – tuning range trade-off. Finally, an improvement of 2 dB in terms of phase noise is achieved by including a by-pass capacitor Cbp. Note that occasionally, depending on the biasing methods of the entire circuit, this capacitor may even impair the phase noise.

The oscillation swing has to be fed out of the circuit, and to maintain a high tuning range and low phase noise, the output should not load the oscillator too much. Furthermore, sufficient isolation should exist between the oscillator and the load, which may vary or be strongly nonlinear. The three alternative output nodes are 1) the resonator itself 2) the bases of the oscillating transistors, and 3) the emitter nodes. Connecting a voltage follower directly to the resonator is widely used but has a severe drawback: the base-collector junction of the input

transistor in the voltage-follower is biased to V_{BC}=0V. Hence, during the oscillation swing the junction becomes forward-biased and it contaminates the phase noise characteristics. The emitter follower can be AC-coupled via a capacitor and biased independently so as to avoid this. Now the drawbacks are the parasitic capacitance of the coupling capacitor and the increased die area. If the output is taken from the base of the oscillating transistor, the coupling capacitor is omitted. In a sense, the decoupling capacitors that already exist are just re-used. Adding the emitter degeneration resistors enables us to take the oscillator signal from the emitter nodes. The voltage swing at the emitter is large enough for the node to be used as an output node. This output configuration does not load the resonator and offers exceptional isolation. Furthermore, the component counts and current consumption are reduced.

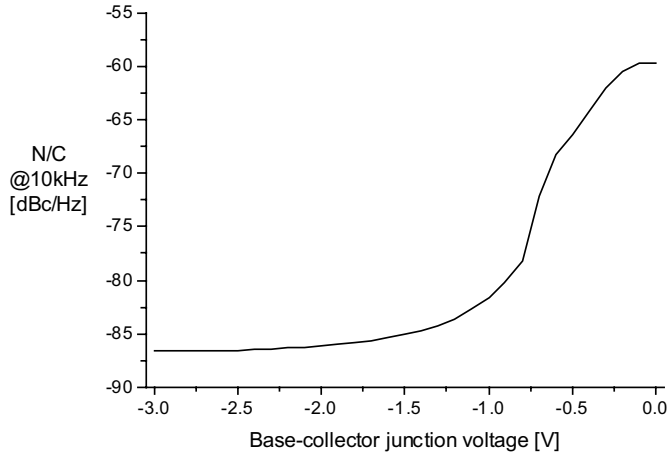


Figure 9.28. Simulated phase noise vs. bias point ($V_{BC} = V_{bias} - V_{supply}$).

On the basis of the previous ideas, four wide-band dual-VCOs were designed. The circuits use the two depicted structures and have either single-ended or balanced coils:

DualVCO1 has single-ended coils and the circuit schematic is depicted in Figure 9.26.
DualVCO2 has a balanced coil and the circuit schematic is depicted in Figure 9.26.
DualVCO3 has single-ended coils and the circuit schematic is depicted in Figure 9.27.
DualVCO4 has a balanced coil and the circuit schematic is depicted in Figure 9.27.

All four dual-VCO circuits include two tunable oscillators and a buffer-amplifier is used to combine the oscillators and isolate them from a load. The two oscillators in each dual VCO differ only in their inductance value, which is used for tailoring the oscillators to the correct frequency band. An external bias current is used for selecting the active oscillator. The buffer is biased from the active oscillator and the other branches are inactive. All four dual-VCOs were on the same die. A microphotograph is presented in Figure 9.29. The circuits were bonded to SSOP36 packages. Two different bonding schemes were used, and correspondingly, *DualVCO1* and *DualVCO4* were on one package type and *DualVCO2* and *DualVCO3* on the other. The measured results are summarized in Table 9.7. In order to avoid duplication, no figures are depicted here, since the *TripleVCO* described later resembles these circuits, and there we will have some detailed figures on the measurement results.

The measured oscillation frequencies were lower than the simulated ones. The fabricated die included some test devices, and these were measured and modeled to find out if this frequency shift is due to improper coils or varactors. The varactor diode used in all the oscillators was based on a npn-transistor with the base and collector connected together, and thus, a reverse-biased base-emitter junction was used as a tunable capacitor. The transistor dimensions were W= 140 μm (40+40+30+30), L= 2 μm. Two such varactors were connected in parallel in a test device. In Table 9.8 the measured and simulated values are compared.

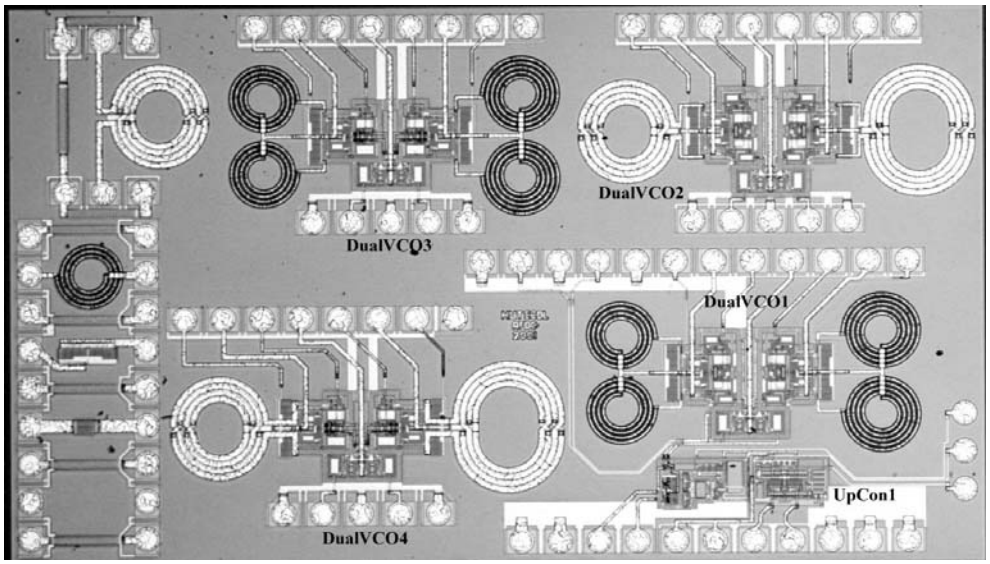


Figure 9.29. Microphotograph of the die fabricated in the fourth run. The die consists of four dual-VCOs, the *UpCon1* upconverter unit, two test inductors, and two varactors.

Table 9.7. Summary of the measured results.

Circuit	I_{DC} [mA]	Freq range [MHz]	Tuning range	N/C@10kHz [dBc/Hz]	FOM
DualVCO1					
Lower band osc.	6.7	1360 – 1690	22 %	-78	173
Upper band osc.	6.6	1720 – 2130	21 %	-83	180
DualVCO2					
Lower band osc.	6.7	1490 – 1840	21 %	-78	174
Upper band osc.	6.6	1800 – 2230	21 %	-80	178
DualVCO3					
Lower band osc.	5.3	1370 – 1730	23 %	-81	178
Upper band osc.	5.3	1730 – 2180	23 %	-79	178
DualVCO4					
Lower band osc.	5.3	1520 – 1890	22 %	-84	181
Upper band osc.	5.3	1840 – 2290	22 %	-80	179

Table 9.8. Measured and simulated test varactor diode characteristics.

	Cap (0-V bias)	Cap (-5-V bias)	Q_{2GHz} (0-V bias)
Measured	4.0 pF	2.2 pF	12
Simulated	3.7 pF	1.9 pF	13

The measured values for a single varactor are 150 fF larger than the ones predicted by the model. Such a small discrepancy is explained by the additional wiring capacitance, process spread, and measurement inaccuracy. As a conclusion, we may note that the model predicts the varactor characteristics accurately. The smaller single-ended and balanced inductors used in the oscillators were also included as test devices. Actually, the dimensions were not exactly the same since the single-ended test inductor was one quarter shorter, and in the balanced test inductor there were two 250-μm long additional feed lines. Accordingly, these were de-embedded. In Table 9.9 the inductor model, EM simulation, and measurement results are

compared. The equivalent circuit model was shown in Figure 5.11. As a conclusion we observe that the EM simulations and measurements agree well.

Table 9.9. Comparison of the inductor model, EM-simulation and measurement results.

	L [nH]	R [Ω]	Cf [fF]	Cp_1 [fF]	Cp_2 [fF]	Rp_1 [Ω]	Rp_2 [Ω]
Single-ended inductor							
Model	2.5	0.75	–	150	150	900	900
EM-sim	3.0	2.5	13	180	190	530	620
Measured	2.9	3	25	180	190	320	460
Balanced inductor							
EM-sim	5.9	4.2	63	100	100	900	900
Measured	5.9	4	60	15	15	800	800

The measured VCO frequency ranges differed significantly from the original simulations. The test device measurements revealed that both the varactor and inductor models are accurate. Neither of these explains the large frequency shift. Instead, the use of the parasitic capacitance extraction tool revealed the reason for the frequency shift. Parasitic capacitances were extracted from the layout using a foundry-supported tool in the Cadence environment. This tool was not available in the first runs, and it was later provided to us as a preliminary-level product. Thus, we had little confidence in its reliability, and therefore this comparison was also performed. Parasitic capacitance extraction was performed for a complete dual-VCO without the inductors. The varactor diode was kept untouched; i. e., the original model was used. The balanced inductor model was based on the measurements. The comparison is presented in Table 9.10, and it shows that with the extracted parasitics the measurement results and simulations agree very well. Therefore, we learnt that the use of this parasitic capacitance extraction tool is a necessity for successful circuit design with this process, and that the tool works properly.

Table 9.10. Post-simulations for *DualVCO2*, upper band oscillator.

Simulation	no layout parasitics	1843 – 2383 MHz
	nominal layout parasitics	1790 – 2217 MHz
	max layout parasitics	1787 – 2206 MHz
	min layout parasitics	1794 – 2227 MHz
Measurement		1800 – 2230 MHz

TripleVCO

In conjunction with the *UpCon2* upconverter, a new oscillator unit was implemented. We learnt from the previous dual VCOs that the layout parasitics reduce the overall tuning range. Therefore, a three-unit VCO bank is required in order to meet the complete frequency range, and this circuit entity is called *TripleVCO*. Its layout was shown in Figure 9.20. The single VCO is based on the same circuit structure as that used in *DualVCO1* and *2,* and that schematic was depicted in Figure 9.26. All the oscillators had the same circuit core and equal varactors, while the EM simulator was used to design the required three coils to set the proper frequency range. The three oscillators within *TripleVCO* are here simply called *VCO1*, *VCO2*, and *VCO3*. Table 9.11 summarizes the measurement results, Figure 9.30 shows typical frequency tuning curves, and Figure 9.31 depicts an example of a "good" phase noise measurement. Here we found out that the oscillators have strange close-in phase noise properties. Figure 9.32 shows

the *TripleVCO* phase noise characteristics at an offset frequency of 10 kHz, and Figure 9.33 shows the phase noise performance at three offsets for *VCO2*. Figure 9.34 depicts the 1/f-noise corner frequencies that were extracted as a function of voltage over the varactor. These measurements indicate that at a large reverse bias for the pn-junction varactors an unknown phenomenon appears. Because of these phase noise problems the varactor leakage current was also measured. According to the device model, the leakage current with a 5-V reverse bias is 20 pA, whereas the measured samples had μA-range leakage currents. Discussions with foundry personnel confirmed that in this particular process run there were severe problems with the quality of the pn-junctions.

Table 9.11. Summary of the measured *TripleVCO* characteristics.

Circuit	I_{DC} [mA]	Freq range* [MHz]	Tuning range	N/C** @1MHz [dBc/Hz]	FOM
VCO1	3.5	1580 – 1874	17 %	-126	178
VCO2	3.5	1869 – 2229	18 %	-125	179
VCO3	3.6	2129 – 2546	18 %	-124	179

* Tuning voltage = 0.25 – 4.75 V ** Measured from the middle of the band, Vtune=3V

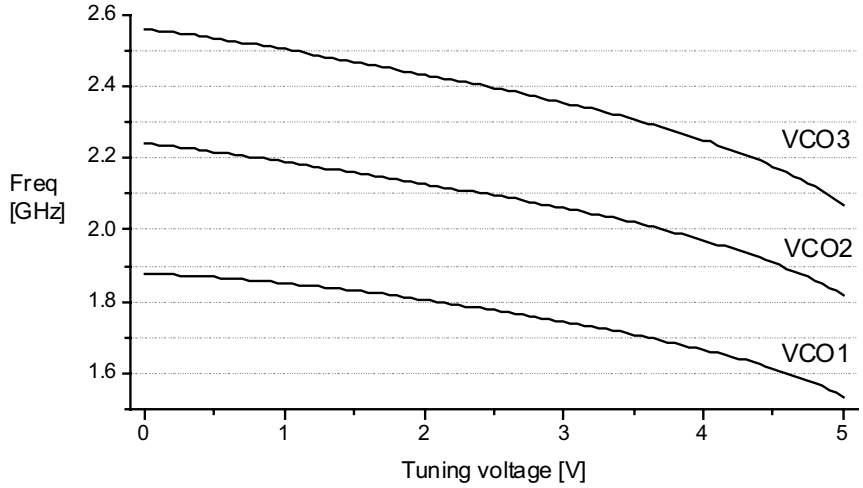


Figure 9.30. *TripleVCO* frequency tuning curves.

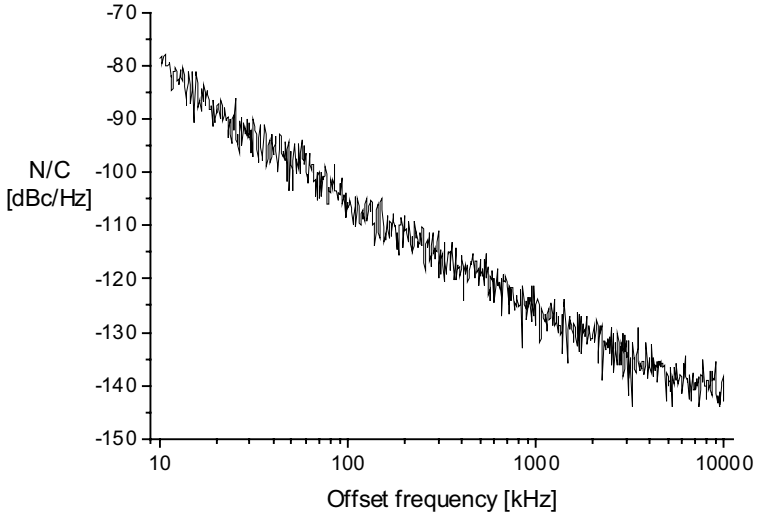


Figure 9.31. TripleVCO phase noise at 2 GHz.

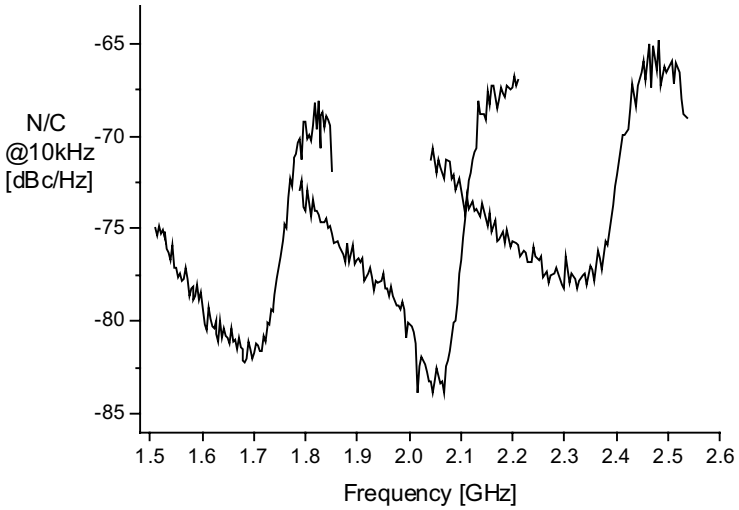


Figure 9.32. TripleVCO phase noise characteristics at an offset frequency of 10 kHz.

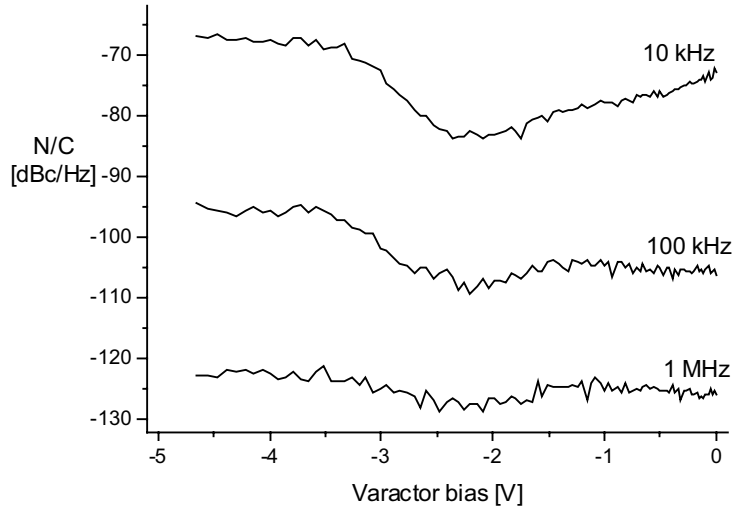


Figure 9.33. VCO2 phase noise characteristics depicted as a function of varactor bias.

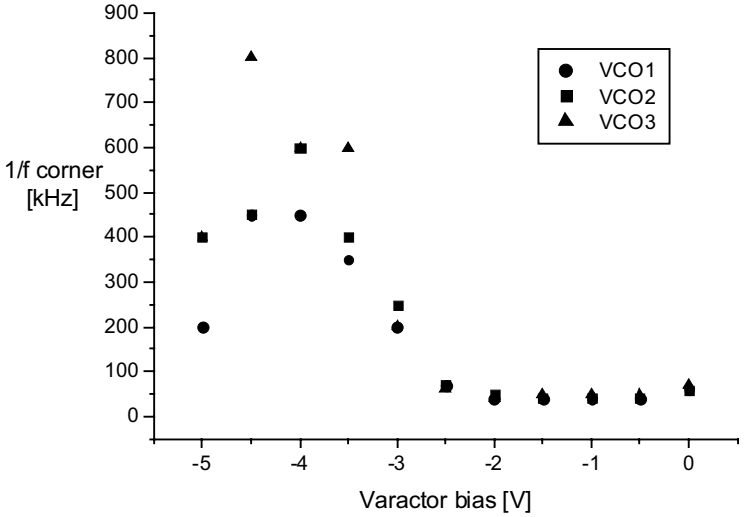


Figure 9.34. Extracted 1/f corner frequencies as a function of varactor bias.

9.4 Flip-Chip VCO Module

The integrated passive device technology (IPD) is a method developed for increasing the integration density, design flexibility, and reliability of an RF module. In such a multi-chip module (MCM) the active elements are either wire-bonded or flip-chip bonded to a substrate that includes high-quality passive devices and interconnection routing. For the sake of convenience, the conceptual structure of the flip-chip technology is illustrated in Figure 9.35. Our industrial partner had developed an IPD technology, and the aim in this project was to gather RF design experience. Oscillators were selected as the research topic simply because it was assumed that they would particularly benefit from the IPD – IC symbiosis. More specifically, in this project we studied the implementation of 4-GHz VCOs using the flip-chip technique for combining a silicon die with an IPD substrate. Furthermore, since this IPD technology was still being developed, our partner was particularly interested in inductor modeling. Therefore, we put a great deal of effort into device modeling, and within this project we developed the automated EM simulation environment, which was described in Section 5.5.3 and in [9.20]. Some of the implemented circuits were published in [9.21].

In the IPD technology that was utilized molybdenum, aluminum, and two layers of copper are fabricated on top of a quartz substrate. The dielectric layers are made of low-loss benzocyclobutene (BCB). In this technology both wire-bonding and flip-chip bonding can be applied to attach discrete devices or ICs. The process offers high-quality inductors, with quality factors at best exceeding 50 at 4 GHz, high-density capacitors, and low sheet-resistance molybdenum resistors, as well as high sheet-resistance thin film resistors. The flip-chip bonding in this project was done by a third party and the flip-chip joints were made of gold, being about 80 μm in diameter and about 30 μm in height. The active devices and varactors were implemented on a low-cost 0.35-μm bulk CMOS technology. The main challenge with this technology was that no RF-dedicated device models were available, and we needed to tailor the models for the RF transistors and for the MOS varactors. Since the applied CMOS technology had a minimum price, and hence a minimum area of 8 mm^2, a set of twelve oscillator cores and a row of test devices were implemented. The implemented die is depicted in Figure 9.36. The die was further post-cut into smaller pieces, and each final silicon chip had a two-by-two matrix of oscillator cores. Such a chip was then flip-chip bonded onto an IPD substrate that included a corresponding arrangement of passive devices. Figure 9.37 shows one such final module that includes four VCOs.

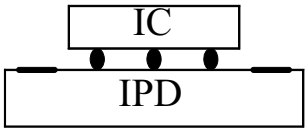


Figure 9.35. Conceptual structure of flip-chip technology.

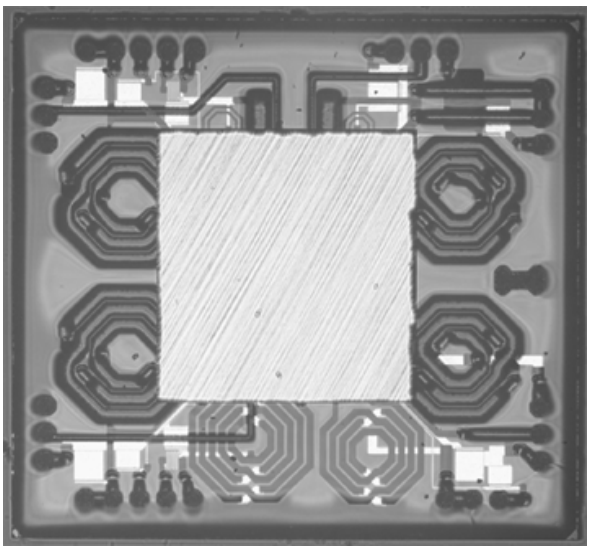


Figure 9.37. Four-circuit CMOS die is flip-chip bonded into IPD substrate.

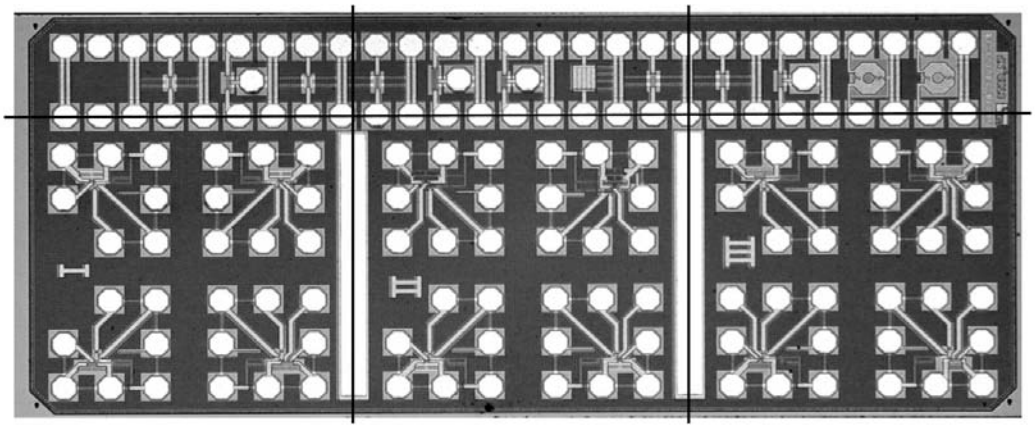


Figure 9.36. Fabricated silicon chip. The black lines indicate how the post-cutting was done.

9.4.1 Circuit Descriptions

The flip-chip technology imposes particular restrictions on VCO topologies. All the active devices and tunable capacitors must be implemented on a silicon die and all the passive devices on an IPD substrate. It is most undesirable to guide the signal back and forth between the IPD and the silicon die, since the size of the module is almost fully dictated by the number of flip-chip contacts. Commonly used topologies, where a cross-coupled MOS pair is fed either with a current sink or source and LC-filtering is used to suppress the phase noise, are therefore not feasible. Furthermore, since in this project the main topic was to gain experience of the use of IPD passives, we obviously selected topologies with many coils. The two basic structures that were selected are depicted with NMOS and PMOS cores in Figure 9.37. CMOS cores were also utilized, and their structures resemble the NMOS circuits with minor differences. In the first topology a conventional cross-coupled pair is biased with a resistor and an additional LC-resonator is used to increase the common-mode impedance of the source node. The resistor biasing is free of 1/f noise and a large capacitor placed across the bias resistor shunts the wideband noise. In the second topology capacitive source degeneration is used [9.22] – [9.24]. The cross-coupled pair is shunted with a floating capacitor Cs. A large bias inductor is used to provide high impedance at the oscillation frequency and at its harmonics. This negative-conductance topology offers reduced parasitic input capacitance, and hence, an increased VCO tuning range [9.21],[9.24]. Furthermore, the circuits included a simple one-stage buffer amplifier. It was specified that a large single-ended output signal should be delivered. Various MOS varactor structures were exploited here with a gate length of 0.5 μm. We used conventional inversion-mode devices, accumulation-mode devices, and motivated by [9.25], we also tested differential structures. Note that in this double-well process accumulation-mode NMOS-devices that have p+ type drain-source diffusions suffer from a DC leakage current from the drain-source node to the substrate. The structures and modeling issues of MOS varactors were thoroughly discussed in Chapter Six, and therefore that topic is omitted here. The characteristics of a 0.5-μm MOS varactor, depicted in Figures 6.12 – 6.15 and listed in Table 6.4, are from the varactors applied in this project, and we may summarize the results by saying that the capacitance values were quite accurate, while the quality factors were really low, only about five at 4 GHz. The inductors and capacitors for the IPD substrate were designed using an EM-simulator. A set of test inductors was fabricated in the same run with the oscillator IPDs and was measured on-wafer. Some of these results were depicted in Figures 5.19 and 5.20. The simulated and measured characteristics agree very well. Typical Q-values for the resonator inductors were about 30. Altogether, twelve oscillators were designed, and here they are named *MVCO1* ... *MVCO12*. Table 9.12 summarizes the structures of the circuits.

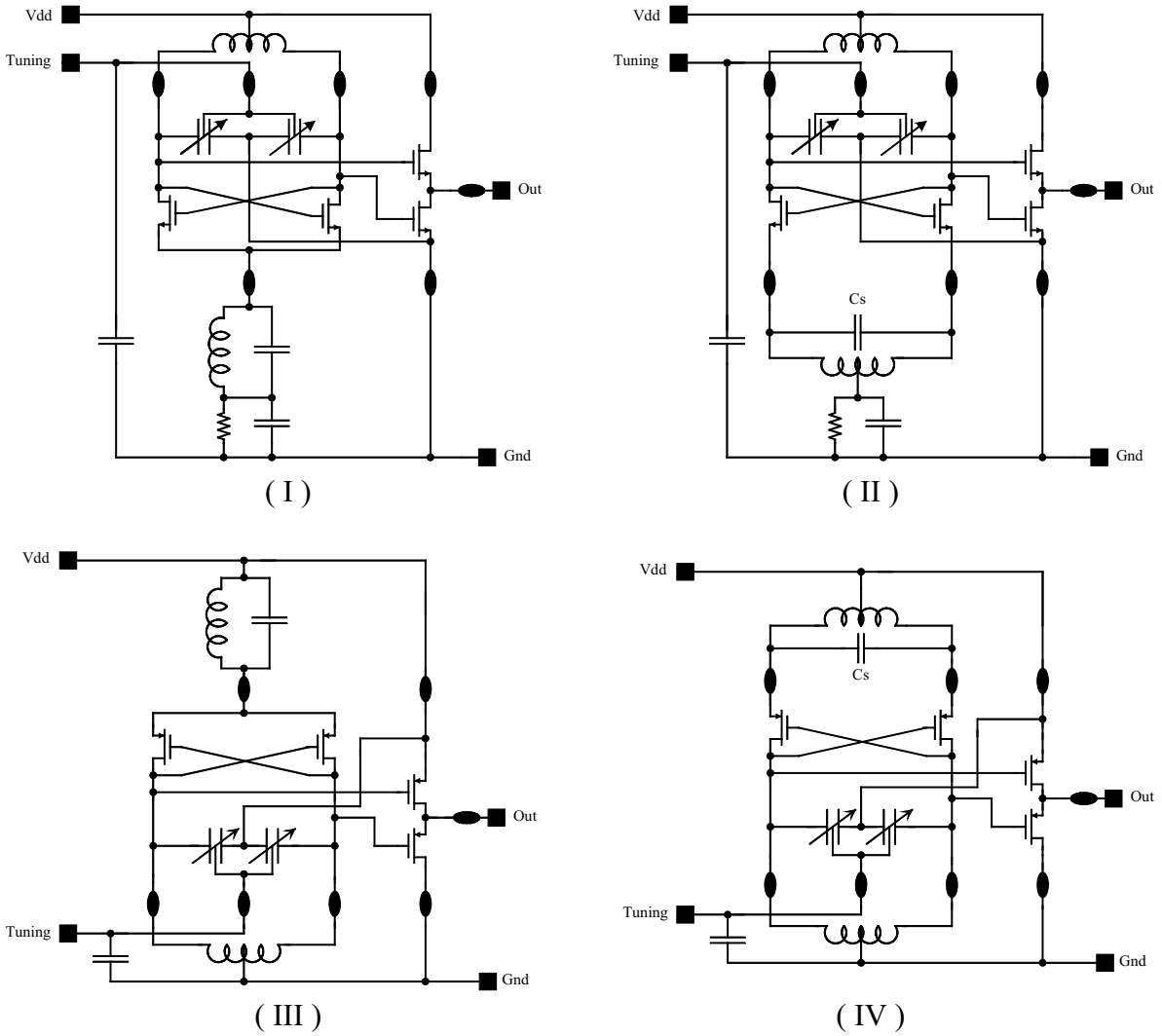


Figure 9.37. Four basic circuit structures: (I) NMOS-CCP with LC-filter (II) NMOS-CCP with capacitive source degeneration (III) PMOS-CCP with LC-filter (IV) PMOS-CCP with capacitive source degeneration. The circular black shapes indicate the flip-chip joints and the squares are for final input/output contacts.

Table 9.12. The implemented circuits.

Circuit	Structure	Core	Varactor
MVCO1	I	NMOS	Inversion-mode NMOS
MVCO2	II	NMOS	Inversion-mode NMOS
MVCO3	III	PMOS	Inversion-mode PMOS
MVCO4	IV	PMOS	Inversion-mode PMOS
MVCO5	I	CMOS	Inversion-mode NMOS
MVCO6	I	CMOS	Inversion-mode NMOS & PMOS
MVCO7	I	NMOS	Accumulation-mode NMOS
MVCO8	II	NMOS	Accumulation-mode NMOS
MVCO9	III	PMOS	Accumulation-mode PMOS
MVCO10	IV	PMOS	Accumulation-mode PMOS
MVCO11	II	NMOS	Differential inversion-mode NMOS
MVCO12	II	PMOS	Differential accumulation-mode PMOS

9.4.2 Measurement Results

The implemented twelve oscillators were measured using on-wafer probes and with an automated measurement sequence programmed by me into an HP4352B PLL/VCO tester. Several samples of each oscillator type were measured and the sample-to-sample spread was fairly small. All the circuits oscillated, but with *MVCO5* a mistake occurred during the design: an error in the IPD layout resulted in the *MVCO5* tuning node not being connected, and thus the VCO did not tune. There were no checking tools available for the IPD layout design. Table 9.13 summarizes the measurement results. The current consumption of each core oscillator is estimated by scaling the measured overall current with the simulated ratio of the core current to total current. Figure 9.38 shows an example of a typical tuning curve, and Figure 9.39 shows a detailed phase noise measurement result. The oscillator circuits with inversion-mode varactors show good performances that are in quite good agreement with the simulations and meet the main targets set in this project.

All in all, in this project we established a good design flow for flip-chip bonded IPD – CMOS IC RF-modules. The EM simulator tool that was developed is able to accurately and efficiently model the passive devices on an IPD substrate. Here we had to choose a relatively low-performance CMOS process, since it was the only one available for us at that time. The implemented oscillators would benefit considerably from a modern CMOS technology with high-Q MOS varactors. The die area on silicon is completely defined by the number of flip-chip joints, and therefore it is not efficient just to have a few active devices on silicon. It would be more attractive to implement slightly more complex circuit, such as a complete PLL, as a RF module using the approach studied here. However, this project was just a one-year project, and despite the promising results it was not continued because of financial issues.

Table 9.13. Measurement results, V_{dd}=2.0 V, V_{tuning}= 0 – 2.0 V

Circuit	$I_{DC,total}$ [mA]	$I_{DC,osc\ core}$ [mA]	Freq range [MHz]	Tuning range	N/C@1MHz [dBc/Hz]	FOM
MVCO1	8	5.2	3460 – 4180	19 %	-126	187
MVCO2	9	6.3	3500 – 4300	21 %	-124	185
MVCO3	10	7.5	3560 – 4250	18 %	-125	185
MVCO4	10	6.4	3640 – 4320	17 %	-125	186
MVCO5	4	1.8	3700	–	–	–
MVCO6	4	2.1	3520 – 4000	13 %	-112	177
MVCO7	8	3.2	3430 – 3530	3 %	-124	187
MVCO8	8	3.5	3330 – 3450	4 %	-123	185
MVCO9	10	6.0	3580 – 3940	10 %	-125	186
MVCO10	7	4.0	3680 – 3980	8 %	-124	187
MVCO11	9	6.3	3300 – 3900	17 %	-120	180
MVCO12	12	7.7	3630 – 4180	14 %	-109	169

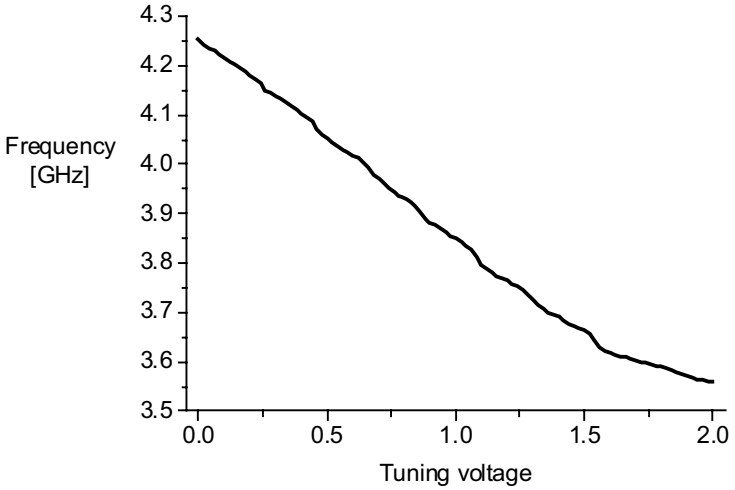


Figure 9.38. *MVCO3* frequency tuning characteristics.

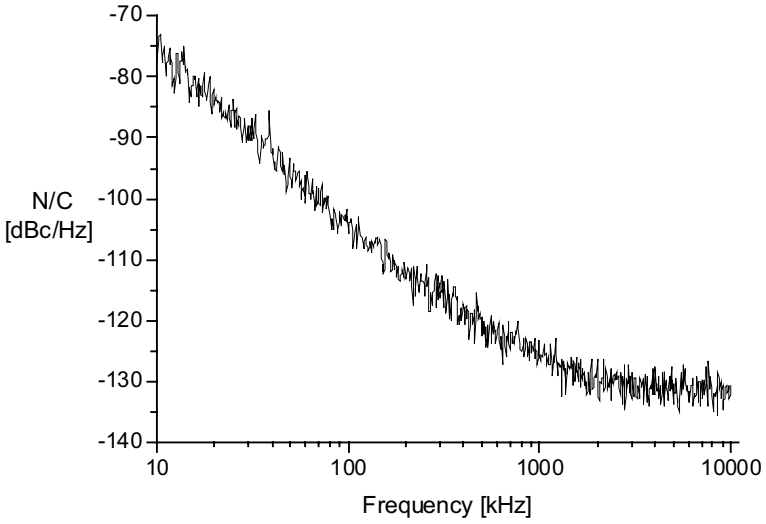


Figure 9.39. *MVCO3* phase noise plot.

9.5 Frequency Synthesizer for WiMedia UWB Radio

Our development work for a UWB transceiver consisted of three phases. First, in the pre-study phase potential circuit techniques for each block in a radio transceiver were studied. In this phase I developed the SSB-mixing based synthesizer plan that was already described in Section 8.3. Two actual circuit design rounds took place. In the second one we had to change the applied process technology, and from the synthesizer design perspective it was therefore almost completely new work, and was actually more demanding than the first round because of challenges with the design kit. Therefore, here too those two process runs are dealt separately in succeeding subsections, and readers should not consider the second one as just an improved version of the first one. Section 8.3 already included a description of the WiMedia UWB standard, and therefore that matter is not discussed further here. As stated there, the SSB-mixing-based synthesizer will most probably suffer from high levels of spurious tones, and therefore we chose to implement a synthesizer based on three parallel phase-locked loops. The synthesizer implemented in the first round was reported in [9.26] and further with an emphasis on PLL issues, in [9.27]. The second circuit was reported in [9.28]. In the first circuit we implemented an RF receiver that included an RF front-end, baseband filters, A/D converters, and the synthesizer unit. The second circuit also included a transmitter unit. Next, the top-level structures of the synthesizer and PLL design issues will be briefly described, while the oscillators and the main RF circuits in the LO path will be described later in slightly more detail.

The implemented synthesizers are based on signal multiplexing. The fundamental idea is quite intuitive and simple. The conceptual structure is presented in Figure 9.40. Three parallel PLLs continuously produce output signals with constant frequencies, and a multiplexer selects one of these at a time. In the first version each PLL included two oscillators, one for band group one (BG1) and the second one for band group three (BG3). Thus, a band group is selected by activating the corresponding VCO in each PLL. In the second version VCOs with a wider tuning range were utilized. The oscillators produce the frequencies for BG3 directly, and the BG1 frequencies are derived with a divide-by-two circuit. Since the required frequencies are constantly present, the frequency-hopping speed is only limited by the inertia of the multiplexer, and therefore this approach offers a very fast hopping speed, just like the SSB mixing method. Since only one frequency output is active at a time, good spectral purity is possible. Each PLL can be designed independently, giving an opportunity to optimize the circuits without compromises with challenging performance demands. Here the PLL settling time is irrelevant, since they boot-up with the complete radio and thereafter just maintain the correct frequency. A set of parallel PLLs has potential drawbacks, mainly in terms of power consumption and die area.

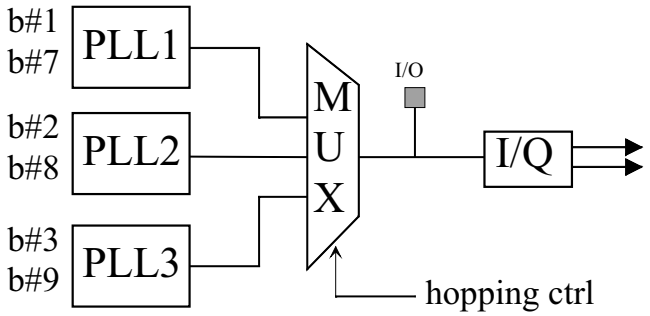


Figure 9.40. Conceptual structure of the UWB LO-generator.

9.5.1 First Synthesizer Implementation

The block diagram for the PLLs applied in the first circuit is depicted in Figure 9.41. All three PLLs operating in both band groups, 1 and 3, can be constructed from a generic integer-N PLL structure, since the desired six output tones can be expressed with $f_{out}=24\cdot11\cdot N_D$. The division count N_D will have one of the values 13, 15, 17, 25, 27, or 29. The reference frequency was chosen to be 11 MHz, and a divide-by-24 prescaler is then needed. The three PLLs differ only in the device sizing within each VCO and in the frequency divider division ratios. Each PLL includes two VCOs, one for band group 1 and another one for band group 3. The band group selection bit is used to activate either the BG1 VCO or BG3 VCO, and to set the corresponding division ratio into the counter. Although each VCO has a slightly different tuning gain and the division ratios differ, the impacts of these variations on the PLL behavior are small enough so for no additional tuning to be needed.

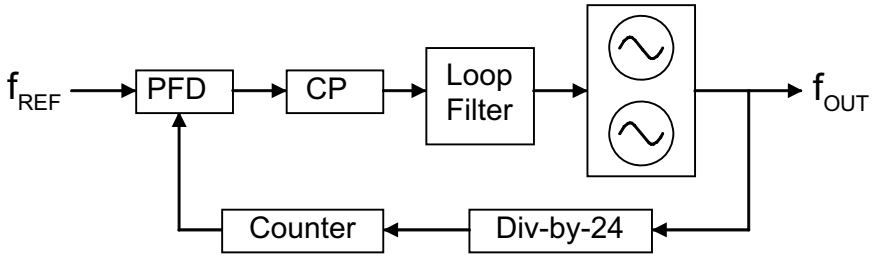


Figure 9.41. PLL block diagram.

The frequency divider consists of a divide-by-24 prescaler and a programmable counter. The counter provides division according to the band group and PLL operating band. Thus, in PLL1, the division ratios are 13 or 25, in PLL2, 15 or 27, and in PLL3, 17 or 29. The prescaler includes a chain of dividers with division ratios of 2, 4, and 3 (2·4·3=24). Furthermore, it includes an additional D-flip-flop (DFF) at the end of the divider chain used for reducing cumulative jitter. All the dividers are based on conventional SCL DFFs that were already discussed in Section 8.1.2. Here, the broad input band poses a design challenge. A lot of power is spent on being able to cope with an input range almost two octaves wide. In the final realization the prescaler consumes half of the total power of each PLL. A simple level shifter is used between the prescaler and the counter, since the logical levels differ. The 5-bit counter was implemented using CMOS logic, and it is able to operate up to an input frequency of 1.5 GHz with nominal device parameters, thus providing a good margin for the required maximum operating frequency of approximately 400 MHz. The counter consumes only 0.1 mW. The low-frequency segment of each PLL consists of a phase-frequency detector (PFD), a charge pump (CP), and a loop filter. The main design issues are a low noise contribution, the low level of the spurious tones, and a small die area. Details of these design issues are given in [9.26], [9.27]. The PFD utilizes a commonly used structure of two DFFs and a delayed feedback containing an OR gate, two inverters, and a 1-pF capacitor. The charge pump is a “switch-in-gate” type circuit so as to be able to operate with a low supply voltage. A fourth-order passive loop filter is used, with a total amount of 126 pF of capacitance, and yet it consumes only about 10% of the total PLL area.

The role of an analog 3-to-1 MUX is to select one of the three PLL outputs at a time and feed it to the poly-phase filter. It has to provide fast switching action, good isolation, and broadband gain. Since strong input signals are continuously present in all three inputs, the isolation is an important parameter for avoiding the mixing of these three signals in the subsequent blocks. A simplified schematic of the MUX and the succeeding buffer is shown in Figure 9.42. The use of the cascode transistor enhances both the isolation and bandwidth. The buffer is a

combination of a voltage follower and a common-source stage with an RC feedback mechanism. It extends the bandwidth compared to a plain source follower and provides a slightly larger output signal.

Quadrature signal generation is accomplished with a three-stage poly-phase RC filter. It offers adequate performance over both band groups 1 and 3, with a sufficient margin for process variations as well. The structure of the PPF and the quadrature signal accuracy that was achieved are illustrated in Figure 9.43. This wideband design of a poly-phase filter motivated us later on to carry out the analysis discussed in Section 8.1.1. The 10-dB loss of the poly-phase filter has to be compensated so as to be able to drive the mixers of the actual receiver chain with an adequate LO amplitude. The buffer-amplifier consists of a resistively loaded common-source stage with a cascode transistor followed by a voltage follower to drive the relatively large input capacitance of the mixer.

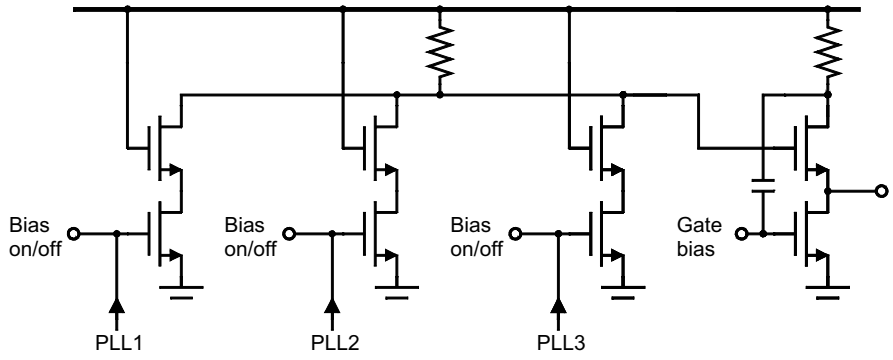


Figure 9.42. Principle of MUX and output buffer. The real circuit is differential and includes biasing circuitry. The active g_m-stage draws 1.2 mA and the buffer-stage draws 1.6 mA.

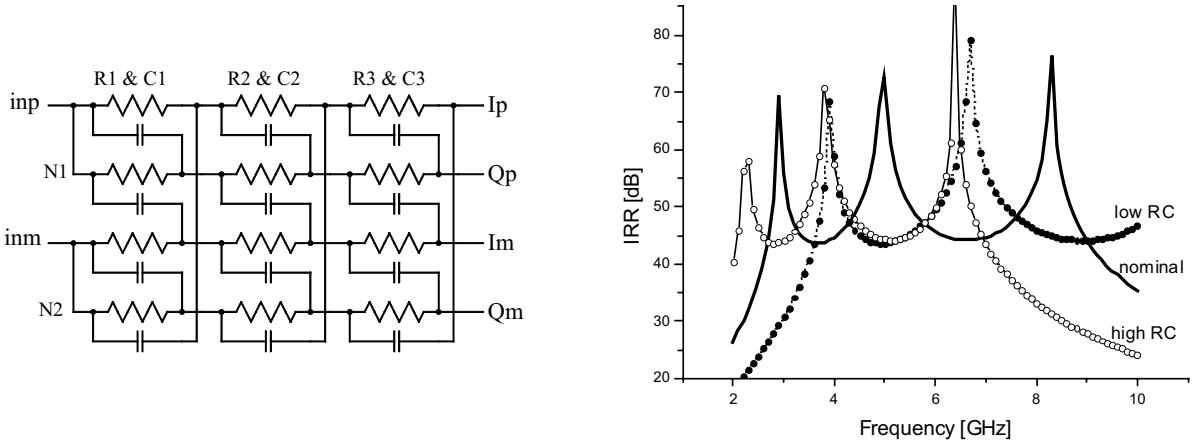


Figure 9.43. (left) Three-stage poly-phase filter. All capacitors are 160 fF, R1=120 Ω, R2=200 Ω, and R3=340 Ω. (right) I/Q accuracy, lines with symbols represent the worst-case process spread. Inside band groups 1 and 3, an IRR of over 35 dB is achieved.

The circuit includes six oscillators, two in each PLL. Since in this application each VCO will only operate at one precise frequency, a very small tuning range could, theoretically speaking, be possible. However, as a result of process, supply voltage, and temperature variations, a sufficient tuning range is needed. With extensive simulations, we found out that an 8-% tuning range is appropriate. All the VCOs have the same topology, depicted in Figure 9.44, and just the device sizes are tailored for the best performance. The outputs of the two parallel oscillators

are fed into a common buffer, which combines the signal routes. Only one VCO in each PLL is active at any time. The VCO circuit includes a cross-coupled NMOS pair for the generation of the negative conductance and an LC resonator consisting of a symmetrical coil and accumulation-mode nMOS varactors. The applied 10-μm width coils have a typical Q_{4GHz}=10. The foundry provided a specific varactor model, and according to this the devices have C_{max}/C_{min}=1.6 and Q_{4GHz}=60. Resistors are used for biasing to avoid the 1/f-noise contribution of a current source or sink. The upper resistor *R1* is the primary bias resistor. Furthermore, another small resistor *R2* at the bottom is used to improve the phase noise characteristics and to provide some isolation to the ground rail. Thus, the VCO floats from both rails and has some immunity to low-frequency disturbances. A PMOS-switch *MP* is used to enable power-down action to take place. It has no significant impact on the VCO characteristics. The capacitor *C1* in parallel with the upper resistor *R1* provides a low-impedance path for the second harmonic, and yet it is so small that low-frequency disturbances in the supply rail do not have an impact on the VCO through this device. According to simulations, the first VCO tunes in 3290 – 3590 MHz within a tuning voltage range of 0.2 – 1.0 V, draws 1.2 mA from a 1.2-V supply, and has phase noise of -118 dBc/Hz at a 1-MHz offset. Correspondingly, the last VCO covers 7380–7950 MHz and draws 2.5 mA, and the phase noise level is -113 dBc/Hz. The buffer consumes about 1 mA.

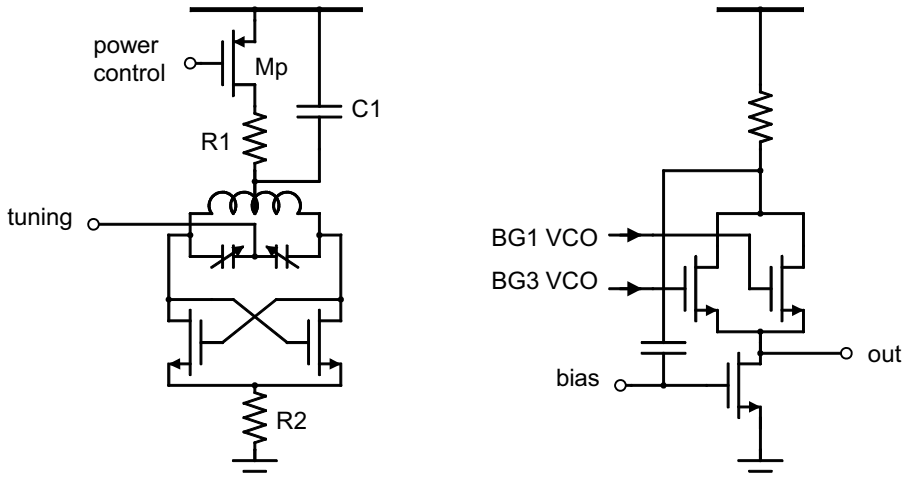


Figure 9.44. VCO and buffer (only one side drawn).

The circuit was fabricated in a 0.13-μm CMOS process, which offers accurate high-quality capacitors and resistors for analog circuits. The LO generator occupies a die area of 1.9 mm^2, excluding the bonding pads. A microphotograph is shown in Figure 9.45. The LO generator had lots of bonding pads and a digital control bus, thus offering an opportunity to measure various building blocks as stand-alone circuits in addition to the complete synthesizer.

The measured tuning curves for the free-running VCOs are depicted in Figure 9.46. The linearity in the actual tuning range (0.2–1.0 V) is very good and does not generate any problems for the PLL dynamics. However, it appeared that the oscillation frequency ranges have been shifted downwards by 6 – 8 %. Recall the simplified design equations for the oscillation frequency and the tuning range:

$$f_{osc} = \left[L\left(C_{\text{var}} + C_{par}\right)\right]^{-\frac{1}{2}} \quad and \quad f_{\max}/f_{\min} = \left[(C_{\text{var,min}} + C_{par})/(C_{\text{var,max}} + C_{par}) \right]^{-\frac{1}{2}}.$$

For the VCO operating in the lowermost band (*VCOb#1*), the simulated center frequency is 3440 MHz and the measured one is 3170 MHz. The discrepancy is 8 %. The simulated tuning

range (f_{max}/f_{min}) is 1.091, while the measured one is 1.092. Since the tuning ranges are still as large as simulated, this shift in frequency cannot be explained by significantly larger parasitic capacitances. During the design we did take into account the additional feed lines from the inductor to the rest of the VCO, and yet the frequency is too low. Furthermore, in the actual receiver chain there was an LC notch-filter, and there the resonance was also shifted similarly. Thus, it seems that there is a problem with the inductor models. Figure 9.47 depicts the phase noise for a free-running VCO. Table 9.14 summarizes the performance of the six VCOs.

Table 9.14. Measured oscillator characteristics. V_{dd}=1.2 V, V_{tuning}= 0 – 1.2 V

Circuit	$I_{DC,\ osc\ core}$ * [mA]	Freq range [MHz]	Tuning range	N/C@1MHz [dBc/Hz]	FOM
VCOb#1	2.0	2980 – 3340	11 %	-115	181
VCOb#2	2.5	3480 – 3900	11 %	-112	179
VCOb#3	2.6	3910 – 4350	11 %	-112	179
VCOb#7	3.4	5830 – 6500	11 %	-105	175
VCOb#8	3.5	6330 – 7030	10 %	-102	172
VCOb#9	3.8	6790 – 7560	11 %	-101	172

* buffer consumes about 1 mA

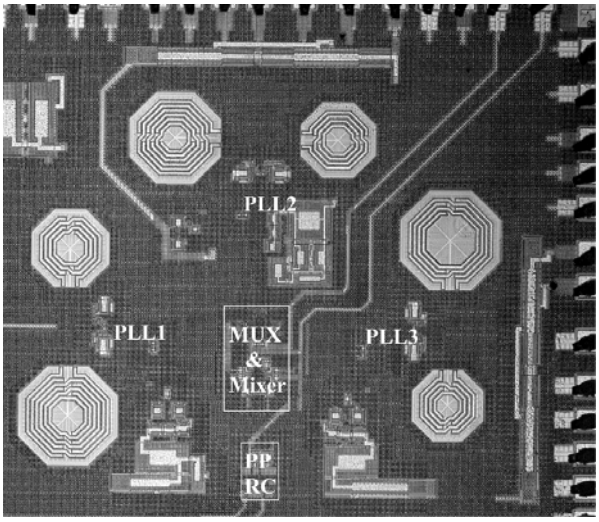


Figure 9.45. Microphotograph of the LO generator. The active area is 1.9 mm^2.

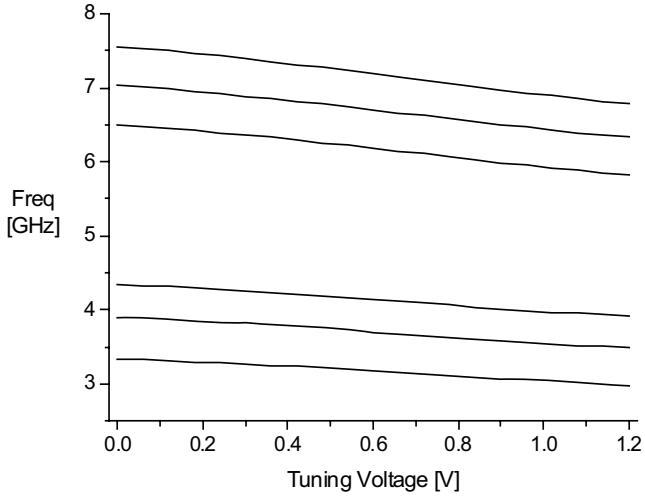


Figure 9.46. Measured tuning curves of the six VCOs.

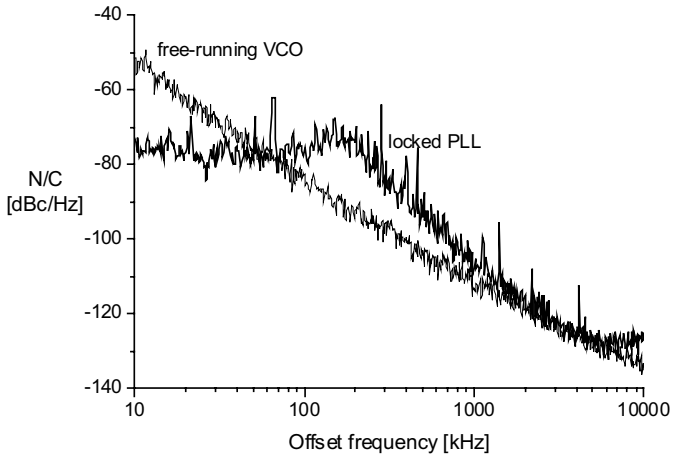


Figure 9.47. Phase noise for free-running VCO and for the locked PLL.

With the use of a 10.3-MHz reference frequency instead of the intended 11.0 MHz, PLLs lock correctly, and thus, despite the shift in the oscillator frequency ranges, we were able to test the complete LO generator. Figure 9.47 also shows the phase noise of the complete PLL. The in-band noise level agrees well with the simulations. The measured close-in spurious tones were higher than those in the simulations by about 10 dB, yet they remain at an acceptable level of about –55 dBc. Figure 9.48 depicts the output spectrum of the LO generator. In this case the operation is in band group three and the MUX output is set to select the PLL2 output. We can observe that $f_{osc}/2$ signal is also present. We do not have any buffer in front of the first divider, and therefore the divided signal that is present inside the first stage of the prescaler leaks backwards into the VCO output node, which is directly coupled to MUX. Furthermore, Figure 9.48 also depicts a clock signal generated on-chip at 1056 MHz [9.26], and how the adjacent UWB LO signals leak through. The adjacent channels leakage is about –30 dBc. The WiMedia UWB standard does not define a maximum level for the adjacent UWB channels, but generally –30 dBc is considered acceptable. All other possible interference tones in the bands of interest are below the measurement noise floor showing over 60-dB purity. Frequency hopping was measured with a 20-Gsa/s digitizing oscilloscope. Figure 9.49 shows a hopping from band 3 to band 1 and the signal recovers within 2 ns. The transitions between the other bands are very similar. The LO hopping was also tested with the complete receiver, and a potentially severe problem, DC-offset accumulation at the baseband output, did not occur.

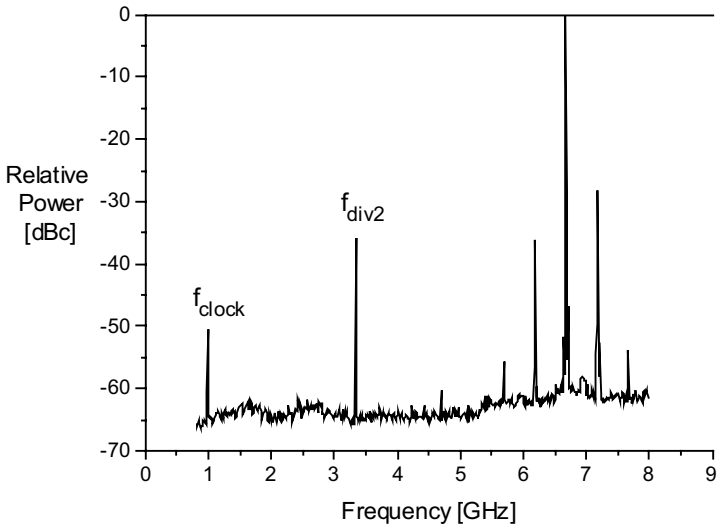


Figure 9.48. LO generator output spectrum.

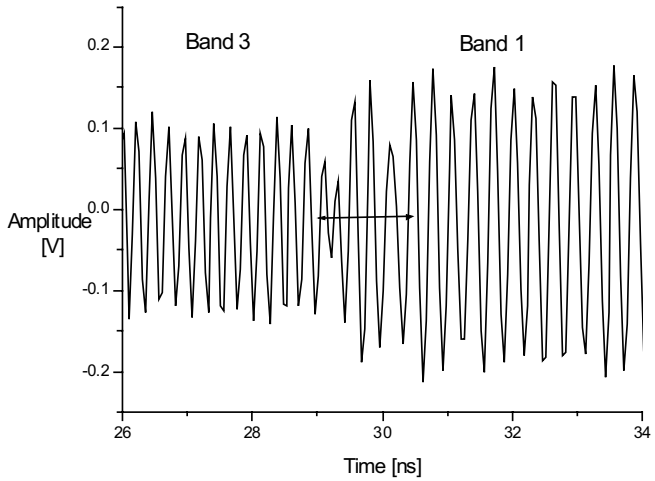


Figure 9.49. Measured LO hopping from band 3 to band 1. Settling time is about 2 ns.

9.5.2 Second Synthesizer Implementation

The large die area was the main drawback of the first version. In this second version the key idea was to reduce the die area by designing oscillators with a wide tuning range for the upper bands and generating the lower bands with a divide-by-two frequency divider. With this approach the lower-band oscillators with large coils are not needed, thus resulting in significant area savings. The new demand is now a VCO with a wide tuning range and yet low phase noise. Table 9.15 illustrates the frequency plan for the second version. The table also includes band group 6 (bands #9, #10, and #11 at 7656 MHz, 8184 MHz, and 8712 MHz). BG6 was considered as a replacement for BG3 in Japan. It turned out that the BG6 LO frequencies can be derived from the existing LO-generator arrangement (BG1 & BG3) with minor modifications and therefore we included it in this new design. Furthermore, we chose to increase the reference frequency from 11 MHz to 66 MHz in order to reduce the in-band noise level and the impact of spurious tones. Hence, the new divider chain includes a divide-by-four prescaler and a 6-bit programmable counter. Although in this design the counter needs to operate with a high-speed input signal, it still consumes only about one mW. Since the PLL parameters changed from the first design, the PFD, CP, and loop filter also required modifications, but those were only minor. Figure 9.50 depicts the structure of the PLLs.

Table 9.15. Frequency plan for the second version of the UWB LO generator.

Operation frequencies			
	BG1	BG3	BG6
PLL1	3432 MHz = ½ · 6864 MHz	6600 MHz	7656 MHz
PLL2	3960 MHz = ½ · 7920 MHz	7128 MHz	8184 MHz
PLL3	4488 MHz = ½ · 8976 MHz	7656 MHz	8712 MHz
Division ratios, reference frequency = 66 MHz			
	BG1	BG3	BG6
PLL1	4 · 26	4 · 25	4 · 29
PLL2	4 · 30	4 · 27	4 · 31
PLL3	4 · 34	4 · 29	4 · 33
VCO frequency range and tuning range (TR) (without safety margin)			
VCO1	6600 – 7656 MHz	TR = 15 %	
VCO2	7128 – 8184 MHz	TR = 14 %	
VCO3	7656 – 8976 MHz	TR = 16 %	

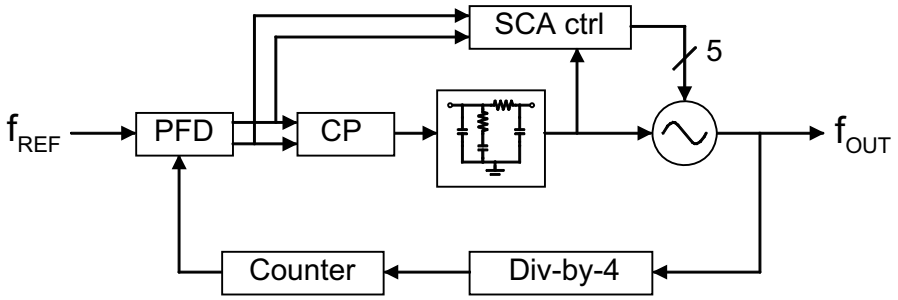


Figure 9.50. PLL structure for the second LO generator implementation.

A VCO with switched-capacitor coarse tuning is needed to achieve a wide tuning range and low phase noise. In order to lock the PLL, the right tuning curve of the VCO has to be found by switching the capacitors in the switched-capacitor array (SCA). The SCA control scheme that is used is based on an architecture where the curve is selected by monitoring the VCO tuning voltage. The SCA control block compares the tuning voltage of the VCO to two reference voltages V_{high} and V_{low}. The comparator outputs are sampled with two D-flip-flops to produce the high and low signals for the state machine, which performs the selection of the tuning curve. A lock detector is used to lock the tuning curve control when the PLL is in locked state. In addition, the digital control bus in the implemented circuit is able to override this control scheme and select one SC curve at a time. This enables detailed VCO characterization to be performed.

The VCO schematic is depicted in Figure 9.51. Each PLL includes one VCO and they are all structurally similar. Only the dimensions of the coils differ. Each VCO consists of an NMOS-CCP with resistive biasing, a 5-bit switched capacitor array for the coarse tuning, an inductor with a symmetrical layout, accumulation-mode NMOS-varactors, and output buffers for feeding the signal into the prescaler and MUX. All the coils are 2-turn devices with metal-six width=8μm and spacing=2μm. According to the device models their inductance values are 0.86 nH, 1.03 nH, and 1.17 nH with Q_{8GHz}=17. The varactor model was provided by the foundry, and according to this model the varactor has a capacitive tuning range of 3.0 with a 1.2-V tuning, Q_{8GHz}= 30, and $C_{0.6V}$= 120 fF. The structure of a single unit in an SCA is shown in Figure 6.23. Because of the parasitic capacitances of the switches, the complete network is not precisely binary-weighed. Instead, the device ratios are 1, 2, 4, 8, and 15. The smallest SCA unit includes only one flux capacitor unit (25.4fF). Since smaller units are not supported in the design kit, this limits the design of the SCA network, i.e., a 6-bit tuning is not feasible. A single SCA unit has a capacitive tuning range C_{ON}/C_{OFF}= 5.5, and Q_{8GHz}=15.

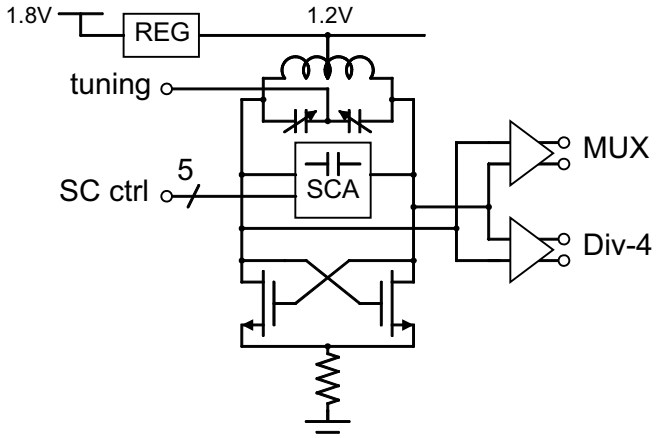


Figure 9.51. VCO schematic.

Finally, Table 9.16 summarizes the main characteristics of the LO generator, and provides a comparison to the simulation results of the first version. The main objective was to reduce the die area, and the die area of the second version is only about one third of that of the first version. The penalty paid for the wider VCO tuning ranges is increased phase noise levels.

Table 9.16. Simulated UWB LO generator performance.

	Version I	Version II
Technology	130-nm CMOS	65-nm CMOS
Output frequencies	BG1 & BG3	BG1, BG3 & BG6
Current consumption	37 mA	66 mA
Active die area	1.9 mm^2	0.6 mm^2
Far-off spurs	< -60 dBc	< -60 dBc
PLL in-band noise	-77 dBc/Hz	-88 dBc/Hz
PLL noise @ 10 MHz	-130 dBc/Hz	-126 dBc/Hz
Frequency settling time (3-MHz hopping)	2 ns	2.5 ns

The circuit was fabricated in a 65-nm digital CMOS process. The process has six metal layers, transistors with three different threshold voltages, high-voltage (1.8-V) transistors, and RF support for interdigitated metal-metal capacitors and symmetrical coils. The change of the process was due to some non-technical reasons, but another motivation was to follow the technology downscaling. The drawback was that this particular process was strongly digitally-oriented, and throughout this second design round we faced severe problems with the design kit. Some analog/RF design tools did not work at all or gave doubtful results, and several updates to the design kit were delivered that included many modifications to the RF device models. This uncertainty was reflected in the final designs, caused a lot of extra work, and is definitely one reason for the unsatisfactory results. A microphotograph of the complete chip is shown in Figure 9.52. The LO generator occupies a die area of 0.6 mm^2. This circuit was measured by bonding it directly to a printed circuit board, and hence in this implementation we had a shortage of interconnections. Therefore, the external VCO tuning was fed with a DC needle into the additional probe pads depicted in Figure 9.52.

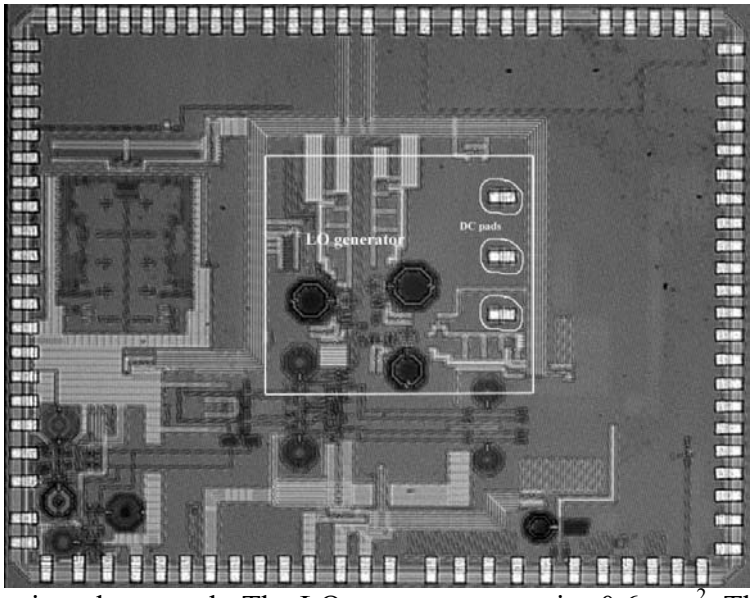


Figure 9.52. Chip microphotograph. The LO generator occupies 0.6 mm^2. The circled pads are used to tune the VCOs in stand-alone measurements.

The PLLs got their supply current through voltage regulators. This regulator was provided to us from an external source, and we relied on that design. It turned out that these regulators suffered from some malfunctions, and therefore the PLLs did not work appropriately. With the full 1.8-V supply the regulators had strange ringing-type behavior around the 66-MHz reference frequency that was used, and the PLLs did not lock properly. When the supply voltage was reduced, so that the regulators were actually just resistors, then some of the other building blocks failed. There was no way to override the regulators. However, we were able to derive some measurement results indicating that the basic functionality of the PLLs and the overall LO-generator are correct. For instance, a 3-ns band-to-band hopping speed was measured. Since full functionality with good results was not achieved, I will just report the measurements of the stand-alone oscillators here. Figure 9.53 depicts the measured tuning curves for *VCO2* and Figure 9.54 shows the phase noise characteristics. In general, all three oscillators have quite a similar performance and the results are summarized in Table 9.15.

Table 9.15. Measured oscillator characteristics. Internal V_{dd}=1.2 V, V_{tuning}= 0 – 1.2 V

Circuit	$I_{DC,\ osc\ core}$* [mA]	Freq range [MHz]	Tuning range	N/C@1MHz [dBc/Hz]	FOM
VCO1	12	5830 – 8850	41 %	-116	182
VCO2	12	6220 – 9480	42 %	-118	184
VCO3	12	6840 – 10400	41 %	-118	185

* Measured value scaled with simulated ratio of core current to total current.

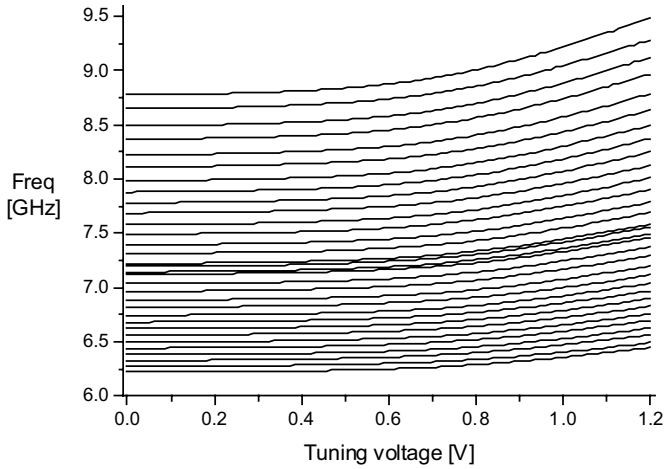


Figure 9.53. Measured tuning curves for *VCO2*.

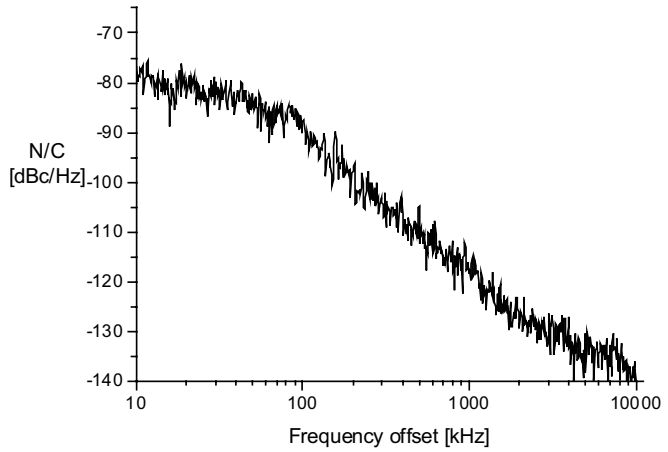


Figure 9.54. Measured phase noise for *VCO2*. The flat region at small offsets is due to the measurement instrument.

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10 Conclusions

In this thesis I have studied the design of integrated LC oscillators and LO signal generation circuits. The research can be divided into three topics: oscillator circuits, the structures and modeling of the LC resonator elements, and the circuits used for frequency conversion or for quadrature signal generation.

Chapters 2 – 4 presented some theoretical background and compared the most common LC oscillators. In the literature a vast number of slightly different circuit arrangements have been proposed, and a question I posed was whether there is a winner among these. In other words, can we find one circuit topology that is superior to all others? The LC oscillator essentially just includes an LC resonator and an active circuit for loss compensation. A well-designed oscillator operates in such a fashion that the active device operates almost like a switch. Therefore, the circuit structure and transistor characteristics have only a small influence on the performance of the oscillator, whereas the quality of the resonator is crucial. Still, this applies only for well-designed oscillators. A poorly designed oscillator circuit typically reveals itself in a high phase noise level, and one may indeed spoil the circuit easily. In oscillator circuits the technology and device characteristics and the performance requirements lead to small variations in the best circuit topology. Therefore, we will continue to see a plethora of oscillator circuit arrangements in the future as well. In particular, oscillators are subject to a phase noise – tuning range – power consumption – die area trade-offs, and that is related to the technology that is applied.

In the mid-1990s, when the silicon RF IC oscillators emerged, there were doubts about the feasibility of these circuits. In particular, the quality of the on-chip passives was poor. The coils had low Q-values and low self-resonance frequencies and the varactors suffered from a narrow tuning range. In some technologies varactors with a high Q-value were available, but in general reducing the losses of the varactors was also a research topic. In this thesis I have presented an analysis of the good structures and modeling issues of the on-chip passives. More than forty test inductors and thirty varactors were implemented and measured. Furthermore, a significant amount of work on the EM simulations of planar inductors was done, and even an automated simulation environment was established. In present-day IC technologies, with their many interconnection layers and nanometer-scale device dimensions, both coils and variable capacitors have reasonably good characteristics. The main issue that is still valid today is the accuracy of the device models, or actually model parameters that are provided by foundries. Both varactors and coils are slightly out of the main stream, and therefore the modeling accuracy, if any models are provided at all, is doubtful. An amusing coincidence in the works of this thesis is that almost whenever I used inductor models provided by a foundry, some problems appeared and the measured results deviated from the simulations. Whenever the coils were modeled by me, either on the basis of simulations or on device measurements, the measured oscillation frequencies were correct. Chapter Seven presented active reactive circuits that are exploited instead of passive resonator elements. Varactors were replaced by tunable capacitors based on the Miller effect or on the current-steering principle. Gyrator-based active inductors were also studied. At first glance these circuits show great promises. Their Q-values are high and tuning ranges wide. However, detailed studies reveal that these circuits suffer from a high level of noise, and the internal signal levels remain low. It is hard to see any use for these circuits, at least not in an oscillator context. A simple ring oscillator also has a wide tuning range and a lower phase noise level, and in particular they are easier to design in a reliable manner.

Chapter Eight presented an analysis of the three commonly used in-phase/quadrature-phase signal generation techniques. The divide-by-two technique and RC polyphase filters were also applied in the actual circuits presented in this thesis. The second topic of the chapter was frequency conversion circuits. System-level considerations were presented to point out the motivation and typical use cases for these circuits. The four mathematical basic operations can be performed for a frequency tone, and these were analyzed in Section 8.2. Two design cases were presented. In the first one I developed a single-sideband mixing method based LO signal generator for WiMedia UWB radio, and in the second one frequency multipliers and a divider were used to extend the frequency range of a digital frequency synthesizer.

Chapter Nine included five sections that presented experimental work done in research projects. The first section presented a temperature-compensated GaAs MESFET VCO and the second project was about passive device and oscillator development with an experimental-level IC process. In the third project we developed a cable-modem RF tuner prototype circuits, and in the fourth project I developed a 4-GHz VCO module with a flip-chip technology. The last project was about a fast-hopping frequency synthesizer for UWB radios. During the work presented in this thesis I have implemented over twenty integrated circuits and seventy passive test devices. I have authored altogether ten journal papers, a thirty conference papers, and two patents.

At the beginning of my work there were doubts as to whether the silicon IC LC oscillators are feasible at all. Passive devices showed poor performance, and the circuit arrangements were also non-optimal. Since then significant improvements have taken place in device performance, in design tools, and in the understanding of oscillator circuits. Nowadays, the LC-VCO can be considered as a similar kind of building block to any other RF IC block. Its design is a challenging yet well-established task. However, in recent years radios have evolved first into multi-band radios, then into multi-system radios, and the next steps are a true software-defined radio and eventually a cognitive radio. In these radios the LO signal needs to span a wide frequency range and change its frequency quickly, and more than one LO signal is needed concurrently. These requirements call for new innovative techniques in LO signal generation and hence this research field will continue to flourish in the future as well.

ISBN 978-952-60-3450-8
ISBN 978-952-60-3451-5 (PDF)
ISSN 1795-2239
ISSN 1795-4584 (PDF)